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Paper No. 17
Entered: December 23, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPENSKY INDUSTRIES, LLC,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2021-01064
Patent 7,725,759 B2

Before THOMAS L. GIANNETTI, BRIAN J. MCNAMARA, and JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

OpenSky Industries, LLC ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting institution of *inter partes* review of claims 1, 14, 17, 18, 21, 22, and 24 ("the challenged claims") of U.S. Patent No. 7,725,759 B2 (Ex. 1001, "the '759 patent"). VLSI Technology LLC ("Patent Owner") filed a Preliminary Response. Paper 9 ("Prelim. Resp."). As authorized, Petitioner filed a Preliminary Reply (Paper 13 ("Prelim. Reply")), and Patent Owner filed a Preliminary Sur-Reply (Paper 16 ("Prelim. Sur-Reply")). As also authorized, Patent Owner filed a Supplemental Brief regarding *In re Vivint, Inc.*, 14 F.4th 1342 (Fed. Cir. 2021). Paper 11 ("PO Supp. Br."). Petitioner filed an opposition brief. Paper 15 ("Pet. Supp. Opp.").

An *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). For the reasons set forth below, we conclude that Petitioner has shown a reasonable likelihood it will prevail in establishing the unpatentability of at least one challenged claim, and we institute *inter partes* review.

A. RELATED MATTERS

The parties both identify the following matter related to the '759 patent: *VLSI Technology LLC v. Intel Corporation*, No. 6:19-cv-00254-ADA (consolidated as 1:19-cv-00977) (W.D. Tex.) (trial concluded with jury verdict). Pet. 5; Paper 5. Patent Owner identifies the following additional matters: *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00057 (W.D. Tex.); *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00299 (W.D. Tex.); *Intel Corp. v. VLSI Tech. LLC*, IPR2020-00498 (PTAB) (on appeal to Federal Circuit,

No. 21-1617); *Intel Corp. v. CLSI Tech. LLC*, IPR2020-00106 (PTAB) (on appeal to Federal Circuit, No. 21-1614). Paper 5.

B. Real Parties in Interest

Petitioner identifies only itself as the real party in interest. Pet. 5. Patent Owner identifies VLSI Technology LLC and CF VLSI Holdings LLC as real parties in interest. Paper 5.

C. The '759 Patent

The '759 patent is titled System and Method of Managing Clock Speed in an Electronic Device. Ex. 1001, code (54). It describes a method of monitoring a plurality of master devices coupled to a bus, receiving an input from a master device that is a request to increase the bus clock frequency, and increasing the bus clock frequency in response to the request. *Id.*, code (57).

D. Challenged Claims

Challenged claim 1 is reproduced below:

1. A method, comprising:

monitoring a plurality of master devices coupled to a bus;

receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

in response to receiving the request from the first master device:

providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and

providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

Ex. 1001, 7:66–8:15. Claims 14 and 18 are independent and recite limitations similar to claim 1. *Id.* at 8:50–9:4, 9:19–40. The other challenged claims depend from one of the independent claims.

E. Prior Art and Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1, 14, 17	103	Shaffer[1], Lint[2]
18, 21, 22, 24	103	Shaffer, Lint, Kiriake[3]
1, 14, 17	103	Chen[4], Terrell[5]
18, 21, 22, 24	103	Chen, Terrell, Kiriake

Pet. 7. Petitioner relies also on the Declarations of Dr. Bruce Jacob. Exs. 1002, 1046.

[1] US 6,298,448 B1, issued Oct. 2, 2001 (Ex. 1005).
[2] US 7,360,103 B2, issued Apr. 15, 2008 (Ex. 1006).
[3] US 2003/0159080 A1, published Aug. 21, 2003 (Ex. 1028).
[4] US 5,838,995, issued Nov. 17, 1998 (Ex. 1003).
[5] US 2004/0098631 A1, published May 20, 2004 (Ex. 1004).

II. ANALYSIS

A. DISCRETIONARY DENIAL

1. Dr. Jacob's Declaration

Patent Owner argues that Petitioner relies on expert declarations filed by Intel in another proceeding. Accordingly, unless cross-examination is available, those declarations are hearsay in this proceeding. Prelim. Resp. 26.[6] The declarations of Dr. Jacob (Exs. 1002, 1046) and Dr. Hall-Ellis (Ex. 1040) were prepared for and filed in two prior IPR proceedings, *Intel Corporation v. VLSI Technology LLC*, IPR2020-00106 (for Exs. 1002 and 1040), and *Intel Corporation v. VLSI Technology LLC*, IPR2020-00498 (for Ex. 1046), (collectively "the Intel IPRs"). The Board denied institution in the Intel IPRs. IPR2020-00106, Paper 17 (denying institution), Paper 22 (denying rehearing); IPR2020-00498, Paper 16 (denying institution), Paper 21 (denying rehearing). Petitioner filed Dr. Jacob's and Dr. Hall-Ellis's declarations here without change, as reflected by the title pages indicating the Intel IPRs. *See* Exs. 1002, 1040, 1046.

Patent Owner argues that Petitioner will be unable to produce either of its declarants for cross-examination, and therefore their statements should be given little weight in this proceeding.[7] Prelim. Resp. 27–29. In that regard, Patent Owner relies on statements in a petition filed by another party, Patent Quality Assurance ("PQA") in IPR2021-01229 ("the PQA IPR"). *Id.* at 27

[6] Fed. R. Evid. 804(b)(1) provides a hearsay exception for former testimony offered against a party who had an "opportunity and similar motive" to develop it by cross-examination. That does not apply here.

[7] Under our rules, cross examination of declaration testimony of retained experts is authorized as mandatory discovery. 37 C.F.R. § 42.51(b)(1)(ii).

(citing IPR2021-01229, Paper 1, 4–5). The PQA IPR does not challenge the '759 patent, but the petition there asserted the existence of an exclusive agreement with Dr. Hall-Ellis. IPR2021-01229, Paper 1, 4. Since filing its petition, however, PQA has corrected itself, confirming that it does not have an exclusive arrangement with Dr. Hall-Ellis. IPR2021-01229, Paper 8, 8 n.2 (stating that the petitioner in that case "erroneously claimed exclusivity with Dr. Hall-Ellis." (citing IPR2021-01229, Ex. 1033 ¶ 9)).

Without any evidence that Dr. Jacob or Dr. Hall-Ellis would be unwilling to testify on behalf of OpenSky, or that PQA asserts a right to prevent them from testifying in this proceeding, we disagree with Patent Owner's assertion that PQA's contentions "make clear that Dr. Hall-Ellis will be unable to testify in this matter and cast significant doubt upon OpenSky's ability to produce Dr. Jacob." Prelim. Resp. 27. In that regard, the facts of this proceeding differ significantly from those of IPR2021-01056, in which OpenSky challenges another one of Patent Owner's patents. While we conclude in that proceeding that the facts support denial of the petition due to the existence of an agreement with PQA preventing Petitioner's proffered expert from appearing for cross-examination, we reach a different decision on the different facts here.

Petitioner contends that it will seek Dr. Jacob's cooperation if trial is instituted. Prelim. Reply 9. While we are somewhat surprised that Petitioner apparently submitted Dr. Jacob's declaration in this proceeding without first seeking this cooperation, on this record we have no reason to think Dr. Jacob would be unwilling to participate, given his prior participation in the Intel IPRs. Of course, under our rules and procedures, Petitioner is responsible for producing Dr. Jacob for cross examination and bears a risk that Dr. Jacob

would not be willing to support the Petition here by appearing for a deposition. *See* Consolidated Trial Practice Guide 23 (November 2019); 37 C.F.R. § 42.53(g) (burden of producing a witness for cross-examination falls on the party presenting the witness).

Petitioner argues that the best approach would be to institute review and consider Patent Owner's objections later. Prelim. Reply 11 (distinguishing cases cited by Patent Owner). We agree that, in some circumstances, Patent Owner's objections may be addressed at trial. For instance, if Dr. Jacob adopts his prior assertions for purposes of this proceeding and undergoes cross-examination, that would allow for a normal discovery process to take place and would require no substantive change to the Petition's contentions.

Because the present record does not indicate that Dr. Jacob would be unwilling to participate in this proceeding or is constrained by a prior agreement from participating, we determine that the best course is to consider the Petition on its merits to determine whether to institute *inter partes* review.

2. District-court litigation

Patent Owner argues that we should deny institution under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). Prelim. Resp. 10–20. The argument is based on a prior litigation in which a jury determined that Intel infringed the '759 patent and that the patent was not shown invalid over "the Yonah Processor" ("the Intel litigation"). Ex. 1027 (March 2, 2021, verdict).

Patent Owner addresses each of the *Fintiv* factors for evaluating parallel litigation involving the challenged claims. *See* Prelim. Resp. 11–20.

Petitioner submits that the factors have limited applicability here, where Petitioner is not a litigation party. Prelim. Reply 6.

Because the Intel litigation is complete, there is no possibility of a stay. *See* Prelim. Resp. 11. Similarly, the Intel litigation has a known outcome and investment. *Id.* at 11–14 (discussing *Fintiv* factors 1, 2, and 3). On the other hand, the only invalidity basis presented to the jury does not overlap with the grounds here, and Petitioner was not a party in the Intel litigation. *Id.* at 14–17.

In our view, Petitioner correctly emphasizes *Fintiv*'s language noting that the Board generally disfavors discretionary denial when litigation did not involve the petitioner, unless "the issues are the same as, or substantially similar to those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal." *Fintiv*, IPR2020-00019, Paper 11, 13–14. Indeed, in multiple decisions Patent Owner cites for support, the Board determined that instituting review would require resolving issues that would also have been resolved by a district court. *E.g.*, *Fitbit, Inc. v. Philips N. Am. LLC*, IPR2020-00828, Paper 13, 15–16 (considering the patent owner's litigation with a non-petitioning party that would overlap with the *inter partes* review at issue); *Mylan Labs. Ltd. v. Janssen Pharmaceutica N.V.*, IPR2020-00440, Paper 17, 19–23 (same, and additionally considering litigation involving the petitioner).

Here, because the Intel litigation did not resolve issues presented by this proceeding, there is no chance of an inconsistent outcome. Indeed, "redoing the work of another tribunal" would only arise when that tribunal has resolved a dispute at issue before the Board. Patent Owner has not argued that resolving a dispute in this proceeding would conflict with an

aspect of the Intel litigation. Thus, we do not agree with Patent Owner that, because "the [litigation] parties and the District Court invested enormous amounts of time and money litigating validity and infringement issues relating to the '759 patent," instituting review here would mean redoing the work of another tribunal. Prelim. Resp. 17.

Patent Owner argues that instituting review here would lead to harassment of Patent Owners who prevail at trial, and that such an outcome fundamentally conflicts with Board precedent and policy. *Id.* at 18. We do not agree that prevailing in litigation against one party should insulate a patent owner from challenge by a different party based on grounds that were not resolved in the litigation.

Considering all of the *Fintiv* factors, we are persuaded that we should not exercise our discretion to deny institution in light of the Intel litigation.

3. Prior petitions

Patent Owner argues that we should exercise discretion to deny institution because the Petition presents the same challenges as prior petitions for which the Board denied review. Prelim. Resp. 20–26. In that regard, Patent Owner relies on the framework from *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential).

As discussed above, the Board denied institution in the Intel IPRs. Importantly, however, it did so based on parallel district-court litigation. *See* IPR2020-00106, Paper 17, 4–13; IPR2020-00498, Paper 16, 4–10. Neither denial considered the merits of Intel's challenges.

Factor 1: whether the same petitioner previously filed a petition directed to the same claims of the same patent

"[W]hen different petitioners challenge the same patent, we consider any relationship between those petitioners when weighing the *General Plastic* factors." *Valve Corp. v. Elec. Scripting Prods. Inc.*, IPR2019-00062, Paper 11, 9 (Apr. 2, 2019). In *Valve*, however, the petitioner and the prior petitioner were co-defendants accused of infringement based on the same product. *Id.* at 9–10. Patent Owner argues that the Board has found a relationship between petitioners when one uses substantive challenges from an earlier petition. Prelim. Resp. 21 (citing *Ericsson Inc. v. Uniloc 2017 LLC*, IPR2019-01550, Paper 8, 12). *Ericsson* imposed a relationship in light of the derivative nature of the petition at issue. *Ericsson*, IPR2019-01550, Paper 8, 12. That decision, however, has not been designated as precedential or informative by the Board, and other decisions have determined that factor 1 weights against discretionary denial for an independent petitioner. *E.g.*, *United Fire Protection Corp. v. Engineered Corrosion Solutions, LLC*, IPR2018-00991, Paper 10 (determining that petitioner independence weighed against discretionary denial, but that substantive similarity with an unrelated prior petition meant the factor only moderately weighed against discretionary denial). We determine that factor 1 weighs somewhat against discretionary denial because Petitioner has not filed a prior petition, but did copy its substantive grounds from a prior petition.

That the Board has not substantively addressed the merits of the prior petitions, in our view, weighs against discretionary denial, because that approach best balances the desires to improve patent quality and patent-system efficiency against the potential for abuse of the review process by

repeated attacks on patents. *See General Plastic*, IPR2016-01357, Paper 19, 16–17. We view substantive consideration as an important factor in that balance, because to determine otherwise would asymmetrically insulate patent owners from potential abuse without addressing the desire to improve patent quality. Patent Owner suffers no abuse from having this tribunal consider the merits of these grounds for the first time.

Factor 2: whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it; and
Factor 4: the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition;

Patent Owner argues that the public was on notice of the grounds asserted in the Intel IPRs, and that OpenSky has thus not offered an adequate explanation of waiting to file the Petition here. Prelim. Resp. 22–23. Petitioner submits that neither it nor any associated persons knew of Intel's petitions or litigation until after the March 2021 verdict. Prelim Reply 4.

We recognize that OpenSky was not formed until after the Intel litigation verdict, but agree with Patent Owner that OpenSky's members' knowledge before forming the entity is nonetheless relevant to our inquiry. *See* Prelim. Sur-Reply 5–6. Petitioner's declarant states that "[n]o person affiliated with OpenSky was aware of the dispute" between Intel and Patent Owner, or aware of the Intel IPRs. Ex. 1048. Without some factual support calling those statements into question, we decline to conclude Petitioner should have known about the art it asserts. Although Patent Owner questions the declaration that OpenSky uses to establish its knowledge, we do not agree that the Board should infer an individual's knowledge based on

unrelated business associations with other individuals. *See* Prelim. Sur-Reply *id.* at 6 (asserting that OpenSky's declarant, Mr. Larocca, has a business partner in other ventures who was aware of the Intel litigation before the verdict).

We conclude that neither factor 2 nor factor 4 supports discretionary denial here.

Factor 3: whether at the time of filing of the second petition the petitioner already received the patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition

Patent Owner argues that because Petitioner reviewed both Patent Owner's preliminary responses and also the Board's institution decisions from the Intel IPRs, factor 3 strongly supports discretionary denial. Prelim. Resp. 23. We agree that Petitioner benefited from Patent Owner's preliminary response, but Patent Owner has not identified how the institution decisions denying review based on *Fintiv* created any further imbalance. Those decisions did not discuss any substantive aspects of Intel's petitions, and did not allow Petitioner to modify its approach through roadmapping. *See* IPR2020-00106, Paper 17 (discussing only discretionary denial under *Fintiv*); IPR2020-00498, Paper 16 (same).

Petitioner's ability to review Patent Owner's preliminary responses in the Intel IPRs allowed Petitioner to address those arguments before filing the present Petition. It is unclear at this time what, if any, changes were made in response. Although we agree with Patent Owner that the opportunity for roadmapping existed, we are unaware of any actual roadmapping here. We conclude that factor 3 weighs in favor of discretionary denial.

Factor 5: whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent;

Considering two petitions from the same petitioner, or petitions from related petitioners, an additional burden arises from not having a consolidated challenge. We determine that OpenSky has offered a reasonable explanation for the timing of the Petition. Here, it was reasonable for OpenSky to take interest in the '759 patent after a substantial damages award, and choose to challenge the patent at that time. *See* Prelim. Reply 5.

We agree with Patent Owner that Petitioner misstates that the Intel litigation did not involve invalidity of the '759 patent (*see* Prelim. Resp. 24), but significant to our analysis here, that litigation did not involve invalidity based on the grounds in the Petition (*compare* Ex. 1027, 5, *with* Pet. 7). Petitioner's explanation that it learned of the large verdict, formed OpenSky, then prepared the Petition adequately explains the Petition's timing. We conclude that factor 5 weighs against discretionary denial.

Factor 6: the finite resources of the Board; and Factor 7: the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review

Patent Owner submits that the Board has expended sufficient resources reviewing the Intel IPRs, and that we stand at risk for parties "flooding the Board with belated challenges to patents that have already been challenged and/or litigated." Prelim. Resp. 25; *accord* Prelim. Sur-Reply 7 ("The Board already expended extraordinary resources here, and instituting here would flood it with (and subject patent owners to) harassing challenges brought by fly-by-night LLC's facing no threat of

litigation."). That assertion, however, fails to distinguish between the Board expending resources on substantive consideration (which it has not done for the '759 patent) and considering why another forum may be better suited to do so (as in the Intel IPRs). Without any Board proceeding requiring ongoing resources for the '759 patent, we conclude that factors 6 and 7 weigh against discretionary denial.

Summary

Having considered all the *General Plastic* factors, based on the present record, we conclude that most factors support institution whereas only one factor weighs against institution. We therefore determine not to exercise our discretion to deny institution under § 314(a).

4. Consistent exercise of discretion

Patent Owner argues that we should deny institution under § 325(d) because *Vivint* "confirms that denial under § 325(d) is required here." PO Supp. Br. 2. We do not agree.

The Federal Circuit held that "the Patent Office, when applying § 325(d), cannot deny institution of IPR based on abusive filing practices then grant a nearly identical reexamination request that is even more abusive." *Vivint*, 14 F.4th at 1354. It found important that, when the Board denied Alarm.com's IPR petition, the Board considered Alarm.com's earlier petitions and reasoned that "allowing similar, serial challenges to the same patent, by the same petitioner, risks harassment of patent owners and frustration of Congress's intent in enacting the [AIA]." *Id.* at 1353 (quoting IPR2016-01091, Paper 11, 12) (alteration in original) (emphasis omitted).

The facts here are not remotely similar. The Intel IPRs were not denied for abusive filing practices, but rather were denied to avoid overlap with a parallel district-court litigation. *See* IPR2020-00106, Paper 17, 4–13; IPR2020-00498, Paper 16, 4–10. This proceeding involves a different petitioner, which has not before petitioned for review of the '759 patent. Those facts show that this Decision does not involve potentially abusive filing practices by the same challenger, as was at issue in *Vivint*.

Patent Owner has not identified how instituting review would be inconsistent with a prior decision on this patent. As explained above, because the invalidity issues presented at trial were different from those considered in the prior application of *Fintiv*, we reach a different conclusion under that doctrine based on different facts here. Thus, *Vivint* is not germane to our decision.

B. Unpatentability Grounds Including Shaffer and Lint

Petitioner relies on Schaffer for most limitations of claim 1, further relying on Lint to support that a "predefined change in performance is due to loading of the first master device as measured within a predefined time interval." Pet. 22–31. Petitioner first asserts that Shaffer teaches the limitation by disclosing that "the CPU 20 operates at a lower speed when the OS 32 determines that no processing is occurring or has not occurred for a predetermined amount of time." *Id.* at 27 (quoting Ex. 1005, 4:6–8). Petitioner relies on Lint as an alternative to Shaffer's teachings in that regard, submitting that Lint discloses "changing the 'performance state . . . based in part on the data representing the average performance over the previous period of time.'" *Id.* (quoting Ex. 1006, 3:1–7). Petitioner reasons that Shaffer describes a "CPU utilization percentage" and that Lint discloses

a way of calculating that percentage that would allow Shaffer's system "to better interface with processor chips featuring hardware coordination of [performance]-states" by saving power, and that doing so would amount to nothing more than using a known technique to improve similar devices in the same way. *Id.* at 27–30 (citing Ex. 1006, 3:2–7, 2:33; Ex. 1002 ¶¶ 208–226).

1. The prior art's disclosures

Shaffer discloses a "CPU speed control system." Ex. 1005, code (57). "The system includes a programmable frequency synthesizer for providing the CPU and other system buses in the device with a variable clocking frequency based on the application or interrupt being executed by the device." *Id.* at 2:17–20.

Shaffer's Figure 1 is reproduced below:

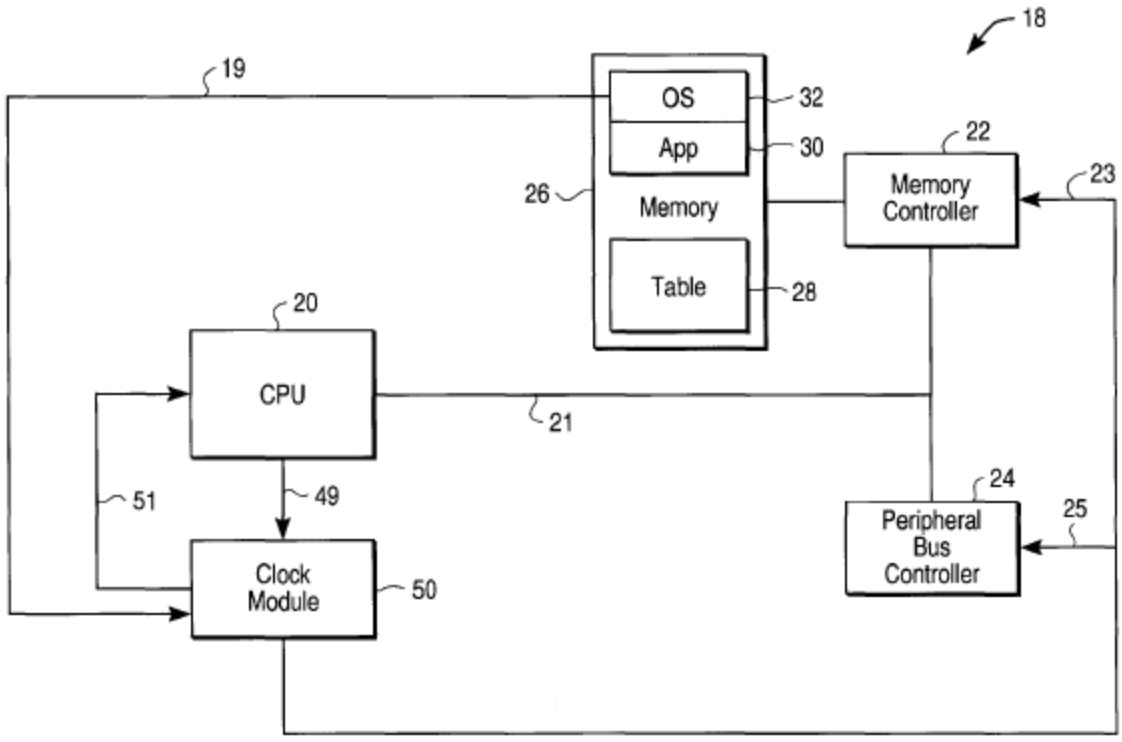

FIG. 1

Ex. 1005, Fig. 1. Figure 1 depicts CPU speed control system 18, including CPU 20 coupled to intelligent programmable clock module 50 such that CPU 20 can instruct clock module 50 to increase or decrease the output frequency as needed, and data/command bus 21 connecting CPU 20 with memory controller 22 and system/peripheral bus controller 24. *Id.* at 3:8–4:25. Shaffer discloses that "when the OS 32 sends a signal to the clock module 50 instructing it to provide the CPU 20 with the clock speed specified . . . both the memory controller 22 and the system controller 24 operate at the specified lower clock speed." *Id.* at 4:41–46.

Shaffer describes that, "in a multiprocessor system (not shown), a separate clock module 50 may be used for each processor, or a single clock

module 50 may drive all the processor clocks." *Id.* at 6:2–5. That same discussion explains that "the CPU and system buses may be clocked using separate clock modules" but that most power savings come from varying CPU clock speed. *Id.* at 6:5–14.

a. Plurality of master devices coupled to a bus

Patent Owner argues that Petitioner fails to show that Shaffer's CPUs, memory controller, and bus controller are master devices. Prelim. Resp. 30–40. First, Patent Owner asserts that because Shaffer does not identify its CPU, memory controller, or bus controller as a "master device," Petitioner's argument is one of inherency. *Id.* at 30–31. We do not agree. Shaffer may use different words to express that those components are consistent with the '759 patent's notion of a master device.

Petitioner notes that a master device may be "a processor, an input/output bus controller, a direct memory access (DMA) controller, an error correction code module or an external memory interface." Pet. 22–23 (quoting Ex. 1001, 3:23–28). We agree with Patent Owner that the patent's statement in that regard does not mean that all instances of the listed types are necessarily master devices. *See* Prelim. Resp. 33–34. But Petitioner relies on more than just falling within one of the possible device types listed by the '759 patent.

Petitioner relies on Dr. Jacob to establish that Shaffer's identified devices are master devices. Pet. 23 (citing Ex. 1002 ¶¶ 229–233). Dr. Jacob explains that Shaffer's "CPU 20, Memory Controller 22, and Peripheral Bus Controller 24 are all master devices, as they are all on the system bus, a shared bus organization (see the *Background* section)." Ex. 1002 ¶ 229 (citing *id.* ¶¶ 53–59). The cross-referenced section explains that a shared bus

permits multiple bus masters where "each bus master (e.g., each CPU or 'processor') is allowed to make its own decisions about when and how to access the shared bus." *Id.* ¶¶ 53, 58. Dr. Jacob states that Shaffer's bus 21 "is a shared-bus organization" with a "system bus controller," and that Shaffer refers to it as "system bus," all indicating that "system bus 21 has multiple bus masters, including the CPU 20, the memory controller 22, the peripheral bus controller 24 . . . , and potentially multiple CPUs." *Id.* ¶ 232.

Patent Owner disputes whether Shaffer discloses multiple master devices. In Patent Owner's view, only CPU 20 is a master device that can request speed changes. Patent Owner submits that because "Shaffer's CPU has a signal line (line 49) to clock module 50 in Figure 1, while controllers 22 and 24 do not," a skilled artisan would understand that the latter devices cannot instruct the clock module 50 to change frequency. Prelim. Resp. 33.

Regarding Petitioner's assertion that Shaffer discloses an embodiment with multiple CPUs, Patent Owner challenges whether disclosing a "multiprocessor" system means the system has multiple CPUs, and whether additional CPUs would be bus masters. Prelim. Resp. 37–38. We disagree with Patent Owner's argument that Shaffer's description of a "multiprocessor" system does not refer to multiple CPUs. Foremost, Shaffer's uses "processor," "microprocessor," and "CPU" interchangeably. *E.g.*, Ex. 1005, 1:38–51, 2:13–15, 2:46–49, 2:53–61, 5:21–30, 5:66–6:14. As noted, Shaffer does not illustrate its described multiple-CPU configuration. But nothing about Shaffer's disclosures are inconsistent with a second CPU mirroring the functionality of the illustrated single CPU. Petitioner asserts that it would have been obvious for a second CPU to be coupled to the same bus as Figure 1's CPU. Pet. 23 (citing Ex. 1002 ¶ 232 ("As the system uses a

shared-bus organization, a person of ordinary skill would understand that any additional CPUs, if present, would be attached to the system bus 21 in the same manner as CPU 20.")). We determine that the record adequately supports Petitioner's contention.

Because Petitioner's contentions regarding Shaffer's multiple CPU embodiment are adequate, we need not determine whether its contentions regarding other possible bus master devices (memory controller 22 or bus controller 24) additionally disclose the claimed "plurality of master devices."

b. Output to control a clock frequency of the bus

Patent Owner argues that Petitioner fails to show the prior art discloses an "output to control a clock frequency of the bus." Prelim. Resp. 40–49. In Patent Owner's view, Petitioner relies on Shaffer's "data/command bus 21" for the claimed bus, but relies on Shaffer's "system bus" for receiving a clock frequency from the clock module. *Id.* at 41–42. We do not agree.

Petitioner cites to Shaffer's disclosures that indicate the clock module provides the clock signal to all of the buses, including the data/command bus 21. For example, Shaffer's Summary of the Invention refers to "other system buses" generically, without mentioning any more-specific bus. Ex. 1005, 2:17–19; *accord id.*, code (57). Shaffer also discloses that the "CPU speed control system 18" provides the clock frequency "to the other controllers and buses in the system" and specifically mentions the "data/command bus 21." *Id.* at 4:15–25. Shafer's statement that "the clock module 50 drives the entire system bus (as mentioned above)" is in the context of alternative disclosures in which separate clock modules may be

achieved to provide different clock signals to the CPU and system buses. *Id.* at 5:66–6:7. That statement does not undermine Shaffer's primary embodiment, in which a single clock signal is provided throughout the system, including "to control a clock frequency of the bus" as claimed.

2. Objective indicia of nonobviousness

Patent Owner submits that the commercial success of its patented invention demonstrates that it is not obvious. Prelim. Resp. 69–71. As evidence, Patent Owner points to the jury's verdict awarding $675 million in damages for the '759 patent. *Id.* at 70.

We do not evaluate Patent Owner's evidence or arguments regarding commercial success at this time. The issue presents a factual issue that Petitioner will have an opportunity to address at trial.

3. Summary

Other than as discussed above, Patent Owner does not challenge Petitioner's contentions for grounds including Shaffer and Lint. Based on the present record, we conclude that Petitioner has shown a reasonable likelihood it will prevail with respect to unpatentability of claim 1 over Shaffer and Lint—Petitioner's showing justifies institution. Pet. 22–31. Our conclusion considers Petitioner's stated motivation for modifying Shaffer in light of Lint.

We have reviewed Petitioner's contentions for claims 14 and 17 as unpatentable over Shaffer and Lint (Pet. 31–33), and for claims 18, 21, 22, and 24 as unpatentable over Shaffer, Lint, and Kiriake (*id.* at 34–39), and reach the same conclusions for those claims.

C. UNPATENTABILITY GROUNDS INCLUDING CHEN AND TERRELL

Petitioner relies on Chen for most limitations of claim 1, submitting that Terrell additionally teaches requesting a clock speed change "in response to a predefined change in performance of the first master device" and that the predefined change "is due to loading of the first master device as measured within a predefined time interval." Pet. 40–49.

Chen discloses an extension to an input/output ("I/O") bus and bridge chip that allows higher speed operation. Ex. 1003, code (57), 1:6–8. To that end, Chen discloses a system "for switching between different data transfer speeds." *Id.* at 1:61–62. Chen's host bridge "interconnects a system bus with an I/O bus" and includes control logic to allow "bus transactions at both a high frequency and a lower frequency." *Id.* at 2:1–6.

Chen's Figure 1 is reproduced below:

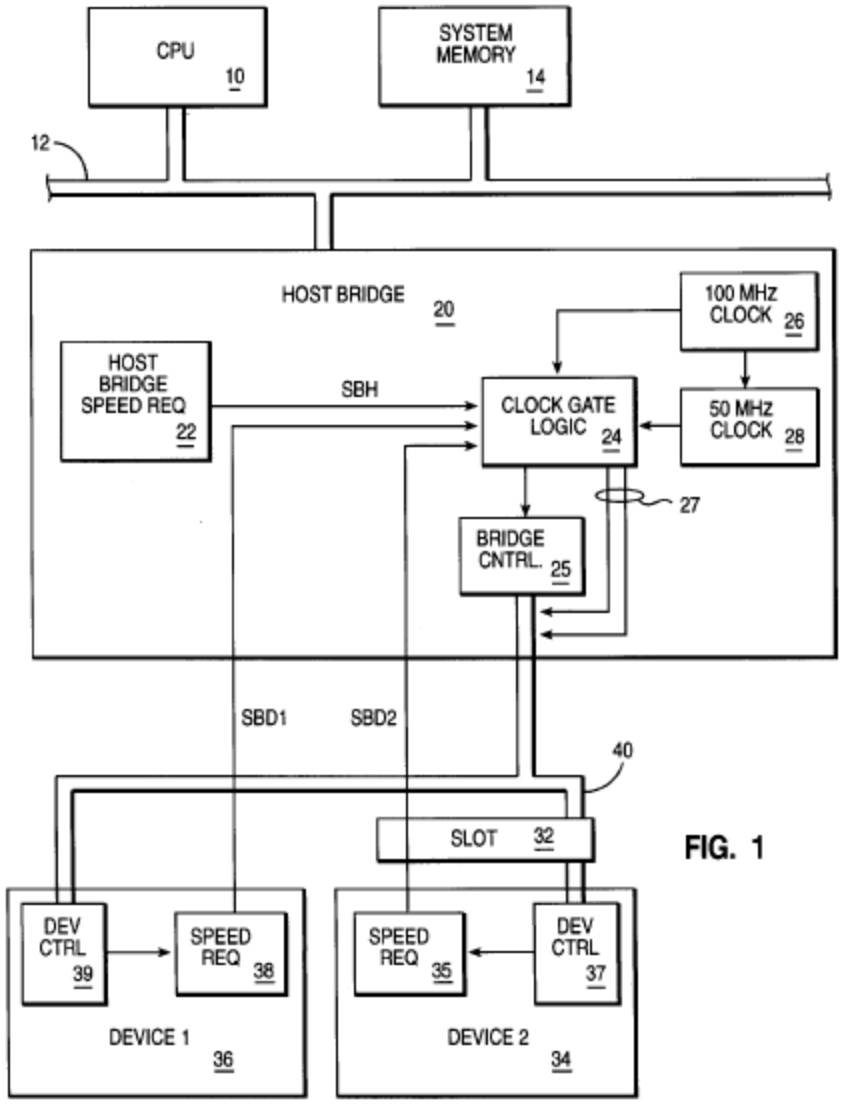

FIG. 1

Ex. 1003, Fig. 1. Figure 1 depicts CPU 10 connected to system bus 12, which connects to host bridge 20, which interconnects system bus 12 with I/O bus 40 that communicates with devices 34 and 36. *Id.* at 2:50–3:4. Device 36 is a "soldered device" while device 34 is a "pluggable device" in slot 32. *Id.* at 3:1–3. Devices 34 and 36 have speed requesting circuits 38 and 35, respectively, that communicate with clock gate logic circuit 24,

which causes the frequency of bus 40 to be dynamically changed through unique clock lines 27. *Id.* at 3:4–22.

Terrell discloses a system and method for controlling the frequency of a common clock shared by a number of processing elements. Ex. 1004, code (57). Terrell states that "it is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the processing elements to function correctly while using the least amount of power." *Id.*, ¶ 5. Terrell states that its goal would be desirable in "[a]n on-chip bus that hosts two or more bus masters, all of which share a common bus clock." *Id.*, ¶ 6.

To implement its approach, Terrell discloses "two basic steps":

> 1. Over a sample period, measure how many clock cycles are being used by each processing element that is attached to the shared clock.
>
> 2. Adjust the system clock frequency to provide the minimum number of clock cycles required by the processing element that is using the largest number of clock cycles.

Id., ¶¶ 25–27.

1. "Providing the clock frequency . . . as an output to control a clock frequency of a second master device"

Patent Owner argues that Petitioner fails to show that Chen discloses "providing the clock frequency . . . as an output to control a clock frequency of a second master device." Prelim. Resp. 50–56. Patent Owner asserts that Petitioner relies on the same aspect of Chen for providing the clock frequency to a second master device and also to the bus, but that Chen does not disclose such dual use. *Id.* at 50–51.

As to providing the clock frequency to the bus, Petitioner relies on Chen's disclosure that, "'[i]n response to' a frequency control signal, 'control logic in the bridge chip causes the higher frequency clock in the bridge chip to be activated such that the host bridge, bus and I/O device are all then operating at the higher frequency.'" Pet. 49 (quoting Ex. 1003, 2:8–14).

As to providing the clock frequency to the second master device, Petitioner relies on Chen's disclosure of a peer-to-peer mode, in which "[b]oth master devices 34, 36 would be provided with the same clock frequency of the high-speed clock (signal of clock line 27) as an output (from clock gate logic 24)." Pet. 48. In that regard, Petitioner cites Chen's statement that "if device 36 requires data from device 34, and both of these devices activate their side band signals (SBD1 and SBD2, respectively), then the data can be transferred at the higher frequency (100Mhz, if both devices are enabled to operate at that speed)." *Id.* (quoting Ex. 1003, 5:61–65). Thus, we do not agree with Patent Owner that Petitioner relies on the same disclosure for both limitations.

But we understand Patent Owner's argument to be that the clock gate logic changes only the bus frequency, rather than also separately setting the frequency of devices 34 and 36. Chen, however, states that the "[c]lock gate circuit 24 causes the frequency of bus 40 to be dynamically changed (gated) by transmitting the appropriate device unique clock lines 27." Ex. 1003, 3:20–22. That indicates that the clock lines 27 are specific to the devices on the bus. Patent Owner argues that, even if lines 27 provide clock frequencies to device 34 and 36, that does not mean the frequencies "'control a frequency of' those devices as claimed." Prelim. Resp. 55 (emphasis

omitted). It is unclear, however, what providing a clock frequency to a device would do besides control its frequency. Similarly, Patent Owner argues that providing devices 34 and 36 with a clock frequency in a peer-to-peer mode would control only the frequency of the data being transmitted between the devices, not the frequency of the devices themselves. *Id.* at 56. Again, Patent Owner does not explain the distinction or why that would be the case.

While Patent Owner has raised reasonable questions regarding Chen's operation, at most those questions identify factual issues appropriate for resolution through trial. The present record supports that Petitioner's showing is adequate for institution.

2. Motivation to combine Chen and Terrell

Patent Owner argues also that Petitioner fails to show skilled artisans would have been motivated to combine Chen and Terrell or that they would have had a reasonable expectation of success if doing so. Prelim. Resp. 56–69.

Patent Owner first challenges whether the Petition adequately justifies using Terrell's teachings to show the limitation "the request sent from the first master device in response to a predefined change in performance of the first master device." Prelim. Resp. 56–57 (citing Pet. 42–47). In that regard, however, the Petition asserts first that Chen alone discloses that limitation because Chen discloses triggering the speed request circuit "when the higher frequency operation is desired." Pet. 42 (citing Ex. 1003, 3:5–13; Ex. 1002 ¶¶ 150, 153). Petitioner points out that a predefined change in performance may include "an event such as a desired increase in device performance." *Id.*

(citing Ex. 1001, 3:64–4:19). That assertion alone appears sufficient to preclude a need to rely on Terrell for this limitation.

As to using Terrell's teachings such that Chen's requests would be sent "based on 'how many clock cycles are being used by each processing element'" (Pet. 44 (quoting Ex. 1004 ¶ 26)), Petitioner asserts it would have been obvious to do so because "[r]educing clock speed was a well-known technique for reducing power consumption." Pet. 44 (citing Ex. 1002 ¶¶ 125–142, 145). While Patent Owner argues that Chen seeks to maximize clock frequency, in opposition to Terrell's goal of minimizing it, we determine that Petitioner has adequately justified the combination. In particular, Dr. Jacob's declaration explains Chen's approach of selecting clock frequency based on the common capabilities of the involved devices, and how that would work with Terrell's approach of determining the performance need by measuring system load. Ex. 1002 ¶ 136. In particular, Dr. Jacob explains the approach of using Terrell's system to determine individual device requirements, which may be reduced because of load, and then using Chen's central arbiter to choose the highest common frequency. *Id.* Dr. Jacob explains that approach "would reduce the clock frequency (and thus the power dissipation, which is a cost) when the system is idle, but if one or more devices are not idle, and therefore likely need more performance, then the clock speed would not be reduced below their needs." *Id.* (emphasis omitted). In our view, that adequately explains how the two approaches would work together. We do not agree with Patent Owner that Terrell's approach is incompatible with Chen's.

Patent Owner disputes certain factual aspects of Chen's system, including whether it discloses a need for lowest-common-frequency

operation. Prelim. Resp. 60 (citing Ex. 1003, 3:5–9, 3:25–29; Ex. 2002 ¶¶ 85–86). In that regard, Patent Owner argues that skilled artisans "would not look beyond Chen for something in Chen," especially where doing so would increase complexity. *Id.* To the extent Patent Owner argues that Chen already has a capability addressed through a combination with Terrell (*see id.* at 60, 63), that does not undermine the combination, because a substitution of one known approach for another may be obvious. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) ("[W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.") (citing *United States v. Adams*, 383 U.S. 39, 50–51 (1966)). And Patent Owner's argument that the combination would unduly increase complexity such that a skilled artisan would not pursue it establishes a factual issue that we decline to resolve on the present record. *See* Prelim. Resp. 64–68.

Patent Owner further criticizes Petitioner's reliance on Terrell's statement that its approach is suitable for applications including an "on-chip bus that hosts two or more bus masters, all of which share a common bus clock." Prelim. Resp. 61 (quoting Pet. 46). Patent Owner asserts that Chen does not describe an on-chip bus, but a peripheral, off-chip bus. *Id.* at 62 (citing Ex. 2002 ¶ 88; Ex. 1003, 3:1–3, Fig. 1). Because of different design constraints for the two bus types, Patent Owner submits that Terrell's statement does not apply to Chen's system. *Id.* at 62–63. In light of our conclusion above regarding Petitioner's primary justification, Patent Owner's argument does not give reason to deny institution. At trial, the

parties will be able to support their contrary views of Terrell's asserted express justification.

Finally, Patent Owner submits that Petitioner has failed to explain why artisans combining Chen and Terrell would have had a reasonable expectation of success. Prelim. Resp. 68–69. That argument appears to rely on the same ideas discussed above, that the two approaches were not compatible and that combining them would have added substantial complexity to the system. *Id.* Dr. Jacob explains why combining Chen and Terrell would have been readily achievable by persons of skill, and in our view that explanation is sufficient. *See* Ex. 1002 ¶¶ 138–139, 143–145.

3. Summary

Other than as discussed above, Patent Owner does not challenge Petitioner's contentions for grounds including Chen and Terrell. Based on the present record, we conclude that Petitioner has shown a reasonable likelihood it will prevail with respect to unpatentability of claim 1 over Chen and Terrell—Petitioner's showing justifies institution.

We have reviewed Petitioner's contentions for claims 14 and 17 as unpatentable over Chen and Terrell (Pet. 49–53), and for claims 18, 21, 22, and 24 as unpatentable over Shaffer, Lint, and Kiriake (*id.* at 54–60), and reach the same conclusions for those claims.

III. CONCLUSION

For the reasons discussed above, we conclude Petitioner has shown a reasonable likelihood of prevailing with respect to at least one claim. We have evaluated all of the parties' submissions and determine that the record supports institution. We conclude that instituting review in this proceeding is

in the interest of efficient administration of the Office and the integrity of the patent system. *See* 35 U.S.C. § 316(b). Accordingly, we institute an *inter partes* review of all challenged claims under all grounds set forth in the Petition.

Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '759 patent is instituted on the claims and grounds set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision.

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