IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	C.A. No. _____ **JURY TRIAL DEMANDED**

VLSI TECHNOLOGY LLC'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff VLSI Technology LLC ("VLSI"), by and through its undersigned counsel, pleads the following against Intel Corporation ("Intel") and alleges as follows:

THE PARTIES

1. Plaintiff VLSI is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of VLSI is Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801. The name of VLSI's registered agent at that address is The Corporation Trust Company.

2. VLSI is the assignee and owns all right, title, and interest to U.S. Patent Nos. 6,212,633 ("the '633 Patent"), 7,246,027 ("the '027 Patent"), 7,247,552 ("the '552 Patent"),

7,523,331 ("the '331 Patent"), and 8,081,026 ("the '026 Patent") (collectively, the "Asserted Patents").

3. On information and belief, Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having its principal place of business at 2200 Mission College Blvd., Santa Clara, CA 95054.

JURISDICTION AND VENUE

4. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over Intel because Intel is incorporated in Delaware. Intel also manufactures products that are and have been used, offered for sale, sold, and purchased in the District of Delaware.

6. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this judicial district because Intel is incorporated in this district, has committed acts of infringement within this judicial district giving rise to this action, and does business in this district.

FIRST CLAIM

(Infringement of U.S. Patent No. 6,212,633)

7. VLSI re-alleges and incorporates herein by reference Paragraphs 1-6 of its Complaint.

8. The '633 Patent, entitled "Secure data communication over a memory-mapped serial communications interface utilizing a distributed firewall," was duly and lawfully issued April 3, 2001. A true and correct copy of the '633 Patent is attached hereto as Exhibit 1.

9. The '633 Patent names Paul S. Levy and Steve Cornelius as co-inventors.

10. The '633 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '633 Patent, including the right to seek damages for past, current, and future infringement thereof.

11. The '633 Patent states that it relates to a "distributed firewall . . . utilized in conjunction with a memory-mapped serial communications interface." Ex. 1 at Abstract.

12. The '633 Patent explains that "Peer-to-peer communications are particularly useful in bandwidth-intensive operations such as video communications. Thus, for example, if a computer CPU is coupled to a video display and a DVD drive through an IEEE 1394 interface, the DVD drive could transmit video information directly to the video display over the interface, thereby eliminating the need for the CPU to process and oversee the transmission." Ex. 1 at 2:51-60.

13. The patent further explains that "one problem associated with . . . memory-mapped communications interfaces, is that there is no provision for secured communications between devices coupled to such interfaces. Each data transmission is broadcast to every node on the interface. Only a node that is indicated as the destination for a data transmission handles the transmission—all other nodes ignore the data transmission. Moreover, data is transmitted without any encryption—a process often used in other environments to scramble transmitted information and thereby prevent unauthorized entities from comprehending any intercepted information." Ex. 1 at 2:60-67.

14. The '633 Patent states that the "distributed firewall incorporates security managers in the selected nodes that are respectively configured to control access to their associated nodes, thereby restricting access to such nodes to only authorized entities." Ex. 1 at 3:52-56.

15. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '633 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products with the infringing features, including Intel products containing Intel On-Chip System Fabric (commonly abbreviated "IOSF") technology.

16. The '633 accused products, for example, embody every limitation of at least claim 36 of the '633 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["A method of controlling access to first and second nodes from a plurality of nodes coupled to one another over a memory-mapped serial communications interface of the type supporting peer-to-peer communications between the plurality of nodes, the method comprising:"]

17. The '633 accused products implement a method of controlling access to multiple IOSF sideband agents (such as the circuit hosting the TMCSRCCLK, TMCSRCCKL2, ENCCKRQ, and ICCSEC registers as described on page 181 of the Intel C620 Series Chipset Platform Controller Hub Datasheet, as well as the "Intel ME" and "PMC" circuits).

5	0h RW/L	**Lock Bit for Group 1 of Dynamically Configured ICC Registers (Lock_ICCG1Dyn):** This lock bit covers registers TMCSRCCLK, TMCSRCCLK2, ENCCKRQ 0: Target endpoint will accept all incoming requests as normal. 1: Target endpoint will deny incoming requests addressed to above listed ICC Registers, unless those requests are attributed with Intel ME SAI or PMC SAI. When denying a request, target endpoint will generate a completion packet as follows: Read will complete without data as Unsuccessful on IOSFSB (normally read completes with data as Successful on IOSFSB), Non-posted Write will complete without data as Unsuccessful on IOSFSB (normally non-posted write completes without data as Successful on IOSFSB) and the Write does not take effect at the register (i.e., register content is not affected.)
4:1	0h RO	Reserved.
0	0h RW/L	**Lock Bit for ICC Security Register (Lock_ICCSEC):** This lock bit covers register ICCSEC, i.e., this same register where this lock bit resides. 0: Target endpoint will accept all incoming requests as normal. 1: Target endpoint will deny incoming requests addressed to ICCSEC register, unless those requests are attributed with Intel ME SAI. When denying a request, target endpoint will generate a completion packet as follows: Read will complete without data as Unsuccessful on IOSFSB (normally read completes with data as Successful on IOSFSB), Non-posted Write will complete without data as Unsuccessful on IOSFSB (normally non-posted write completes without data as Successful on IOSFSB) and the Write does not take effect at the register (i.e., register content is not affected.)

18. This method controls access over a memory-mapped serial communications interface. For example, ICCSEC is memory-mapped at offset 0x1020.

ICC Security (ICCSEC)—Offset 1020h

19. Furthermore, agents on the IOSFSB, which stands for "IOSF Sideband," use serial communications.

20. For example, Intel's U.S. Patent No. 9,213,666 discussing IOSF sideband explains that "[a] sideband interface . . . can be implemented as a serial message interface (instead of many parallel sideband wires) to simplify structural layout requirements." 6:53-56.

21. Moreover, the patent further notes that "on-chip power management control" is an "example[] of communication types that may be sent via a sideband message interface," 6:57-59; "PMC," referenced above in the ICCSEC description, appears to be a type of Power Management Control based on its use of an acronym commonly appropriated for that purpose, further correlating the "IOSFB" reference with IOSF sideband as described in the '666 patent. Similarly, the patent notes that "a manageability engine" (such as Intel's ME) can communicate

through an IOSF sideband hub, further correlating the "IOSFSB" reference with IOSF sideband as described in the '666 patent. 15:19-22.

22. As described in the '666 patent, IOSF sideband can provide communications "between the agents" on the fabric (as stated in the Abstract), *i.e.*, peer-to-peer communication between nodes on the fabric, such as the circuitry implementing ICCSEC, Intel ME, and PMC.

["a) controlling access to the first node using a first security manager disposed in the first node,"]

23. The '633 accused products control access to the first node using a first security manager disposed in the first node, such as the Policy Enforcer 371 in each IOSF sideband agent, such as the circuit implementing the PMC, that controls access to the sideband agent, such as the node implementing registers TMCSRCCLK, TMCSRCCKL2, ENCCKRQ, and ICCSEC.

24. As explained in Intel's U.S. Patent No. 9,805,221 discussing SAI attributes, referenced above in Intel's discussion of ICCSEC in the Intel C620 product, "incoming security information, which can include, in one embodiment, the SAI, command information and address information, can be provided through input multiplexer 376 to policy enforcer 371 to determine whether access is to be permitted," 7:34-39, with reference to Figure 5 reproduced here:

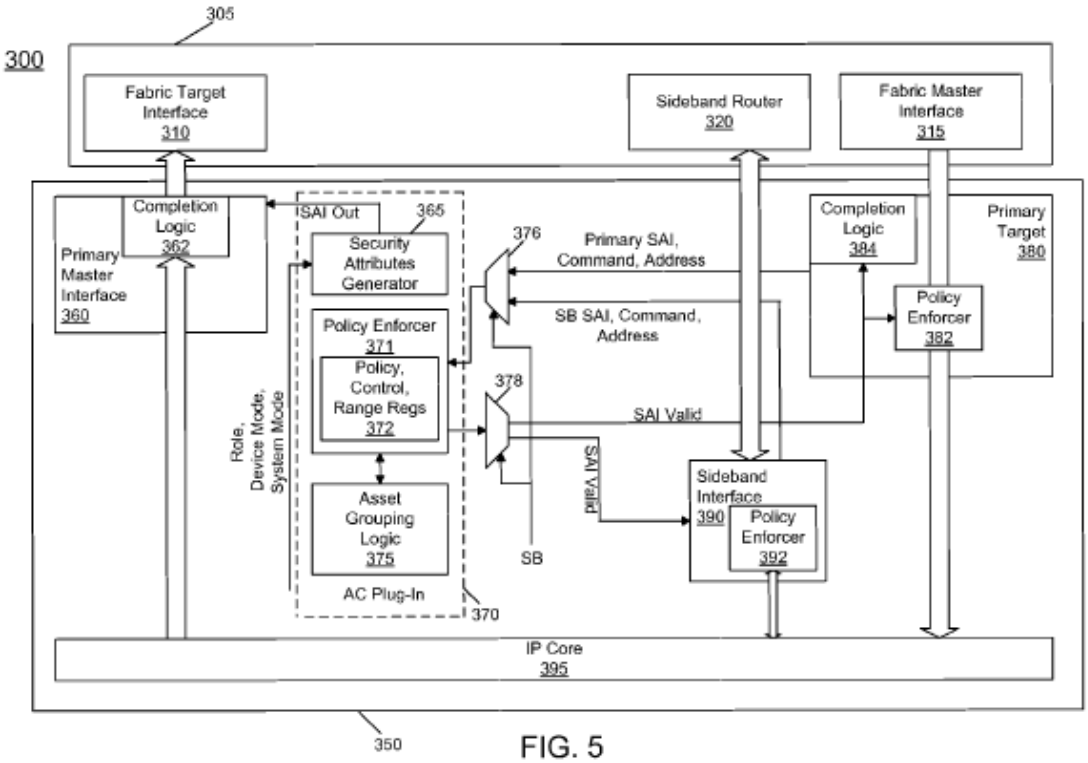


FIG. 5

25. The Security Attributes Generator 365 and the Policy Enforcer 371 present in the IOSF agents (such as the Intel ME, the PMC, and the circuit implementing ICCSEC), are a distributed firewall as claimed.

26. Furthermore, as explained in the '221 patent, functional units "may also be configured to perform sophisticated access control mechanisms such as dynamic policy configuration to enable on-the-fly revision of policy values linked to an asset," thus locally generating an authorization list of authorized nodes as claimed. 8:36-39.

["wherein the first node is assigned a segment of memory addresses for the communications interface, the segment of memory addresses including secure and unsecure portions thereof,"]

27. The first node in the '633 accused products is assigned a segment of memory addresses for the communications interface, the segment of memory addresses including secure

and unsecure portions thereof. For example, as shown in the excerpt from page 181 of the Intel C620 Series Chipset Platform Controller Hub Datasheet above, the Lock_ICCG1Dyn and Lock_ICCSEC bits of the ICC Security register control access to certain memory-mapped ICC registers. For example, Lock_ICCG1Dyn controls access to TMCSRCCLK, TMCSRCCLK2, and ENCCKRQ, and when the bit is 1, accesses are denied. In this configuration, the memory-mapped addresses of these registers (at offsets 0x1000, 0x1004, and 01x1008, respectively) are a secure portion of the segment of memory addresses. Analogously, Lock_ICCSEC controls access to the ICC Security Register mapped at offset 0x1000. When this bit is 0, the memory-mapped address of ICCSEC is an unsecure portion of the segment.

["and wherein the first security manager is configured to control access only to the secure portion of the segment of memory addresses for the first node; and"]

28. The first security manager of the '633 accused products is configured to control access only to the secure portion of the segment of memory addresses for the first node. For example, as explained on the above-referenced page 181, setting the Lock_ICCG1Dyn and/or Lock_ICCSEC bits trigger SAI-based access controls by the Policy Enforcer only in the IOSF sideband agent corresponding to the circuit implementing the relevant registers.

["(b) controlling access to the second node using a second security manager disposed in the second node"]

29. Access to the second node in the '633 accused products is controlled using a second security manager disposed in the second node. For example, other sideband nodes also control access with their own Policy Enforcer circuits using SAIs, as discussed above, such as Intel ME and PMC.

["wherein the first and second security managers define a distributed firewall for the communications interface."]

30. The first and second security managers define a distributed firewall for the communication interface in the '633 accused products. For example, by controlling access to individual nodes as described herein, the Policy Enforcers define a distributed firewall for the IOSF sideband agents.

31. Intel has long had knowledge of the '633 Patent. For example, the '633 Patent has been cited in multiple Intel patent prosecutions, including during the prosecution of its U.S. Patent Nos. 7,215,781; 9,507,962; 9,507,963; 9,547,779; and 9,619,672. To the extent Intel claims it did not have broader actual knowledge of the '633 Patent, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

32. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '633 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States (as used in this pleading, "customers" refers to both direct and indirect customers, including entities that distribute and resell the accused products, alone or as part of a system, and end users of such products and systems). For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '633 Patent. *See, e.g.*, http://ark.intel.com. On

information and belief, Intel's customers directly infringe the '633 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

33. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '633 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '633 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '633 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '633 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '633 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

34. As a result of Intel's infringement of the '633 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

35. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '633 Patent.

36. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

37. VLSI is informed and believes, and thereon alleges, that the infringement of the '633 Patent by Intel has been and continues to be willful. As noted above, Intel has long had knowledge of the '633 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

38. VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

SECOND CLAIM

(Infringement of U.S. Patent No. 7,246,027)

39. VLSI re-alleges and incorporates herein by reference Paragraphs 1-38 of its Complaint.

40. The '027 Patent, entitled "Power optimization of a mixed-signal system on an integrated circuit," was duly and lawfully issued July 17, 2007. A true and correct copy of the '027 Patent is attached hereto as Exhibit 2.

41. The '027 Patent names Marcus W. May and Matthew D. Felder as co-inventors.

42. The '027 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '027 Patent, including the right to seek damages for past, current, and future infringement thereof.

43. The '027 Patent states that it "relates generally to portable electronic equipment and more particularly to a sensing digital and analog parameters of an integrated circuit to provide power supply optimization." Ex. 2 at 1:7-10.

44. The '027 Patent explains "a need exists for an integrated circuit that provides multiple functions through mixed-signal operation and architectures for handheld devices with

appropriate optimized power-consumption and with a minimal requirement of external components." Ex. 2 at 2:32-36.

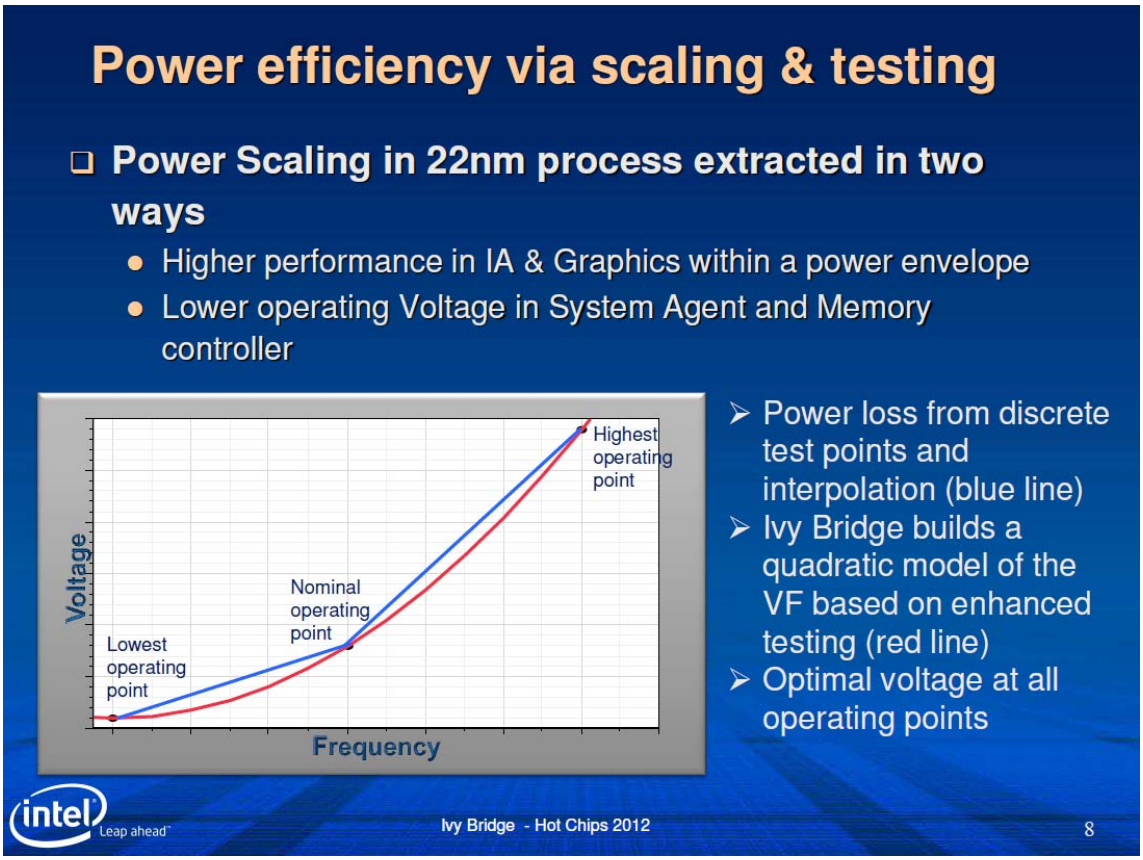
45. The '027 Patent provides "a method and apparatus for conserving power of a system-on-a-chip having analog circuitry. An aspect is a method and apparatus for increasing the power supply efficiency of an integrated circuit, by determining an analog variation parameter that is representative of an integrated circuit fabrication process variance of the integrated circuit. An operational temperature is determined, where the operational temperature is associated with the analog variation parameter. With the analog variation parameter and the operational temperature, an adjustment signal is determined for a power supply level of the integrated circuit, such that power consumption of the integrated circuit is optimized." Ex. 2 at 2:40-51.

46. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '027 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products with a Power Control Unit (PCU) to compensate for Inverse Temperature Dependence (ITD) in an infringing manner.

47. The '027 accused products embody every limitation of at least claim 18 of the '027 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["A method for increasing power supply efficiency of an integrated circuit, comprising:"]

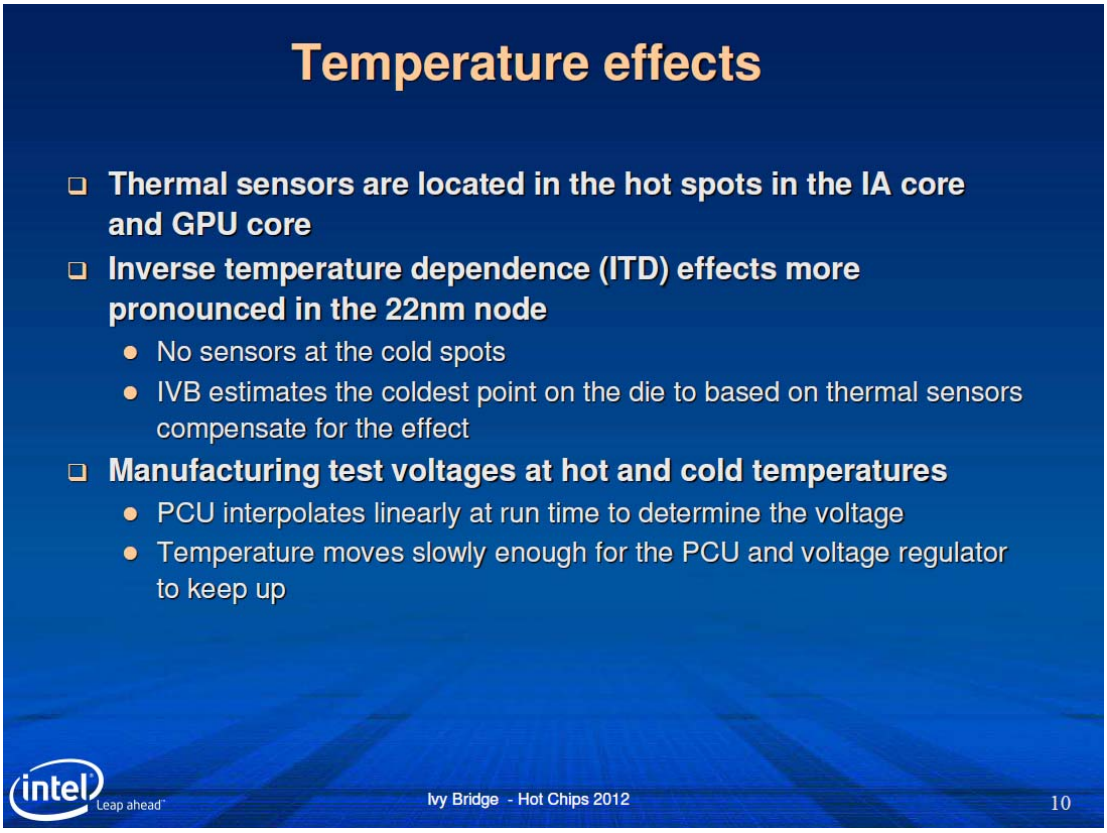
48. The '027 accused products use a method for increasing power supply efficiency of an integrated circuit. For example, the PCU of the '027 accused products is designed to maximize the power supply efficiency of a microprocessor by using the "optimal voltage at all operating points" in a manner such as that shown below.



["determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; and"]

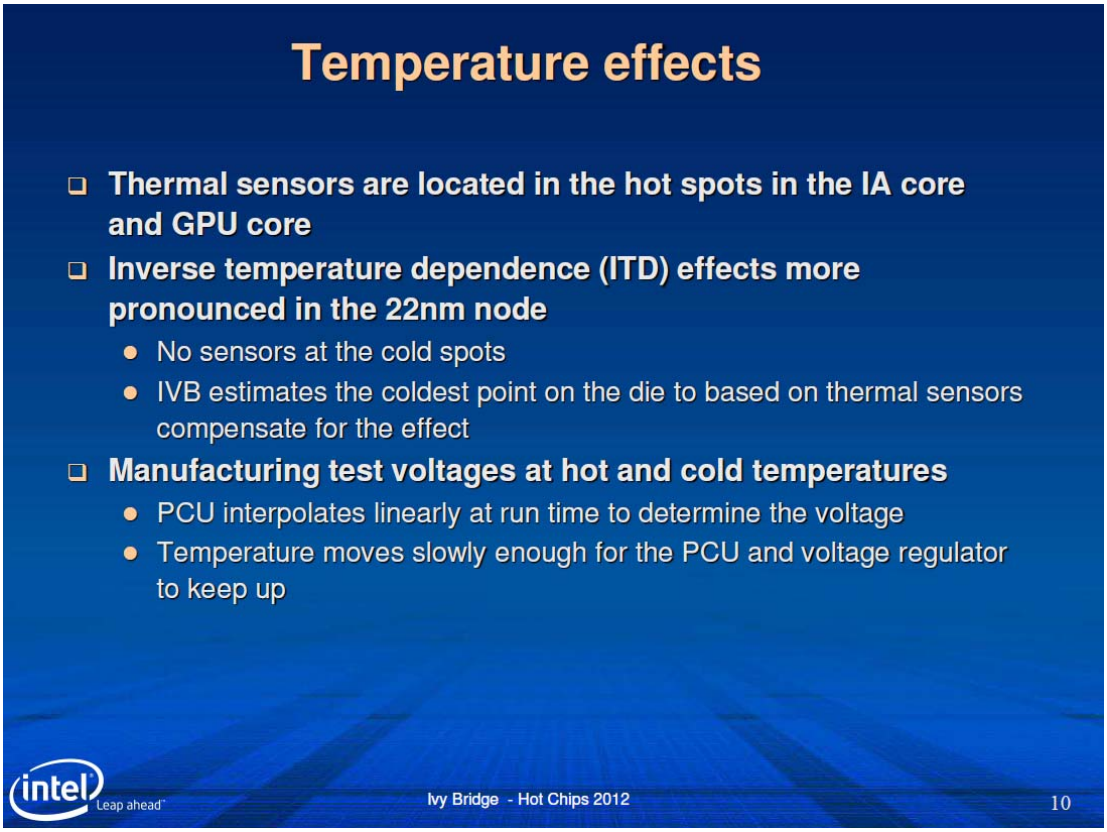
49. The '027 accused products use a method that includes determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit. For example, Intel marketing materials demonstrate that the PCU of the '027 accused products uses thermal sensors to estimate the temperature of the coldest point on the die

to compensate for Inverse Temperature Dependence using a process and architecture such as that described below.



["determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter, and"]

50. The '027 accused products use a method that includes determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter. For example, Intel marketing materials demonstrate that the PCU interpolates linearly against test voltages to determine a power supply voltage level through a process that practices this element.

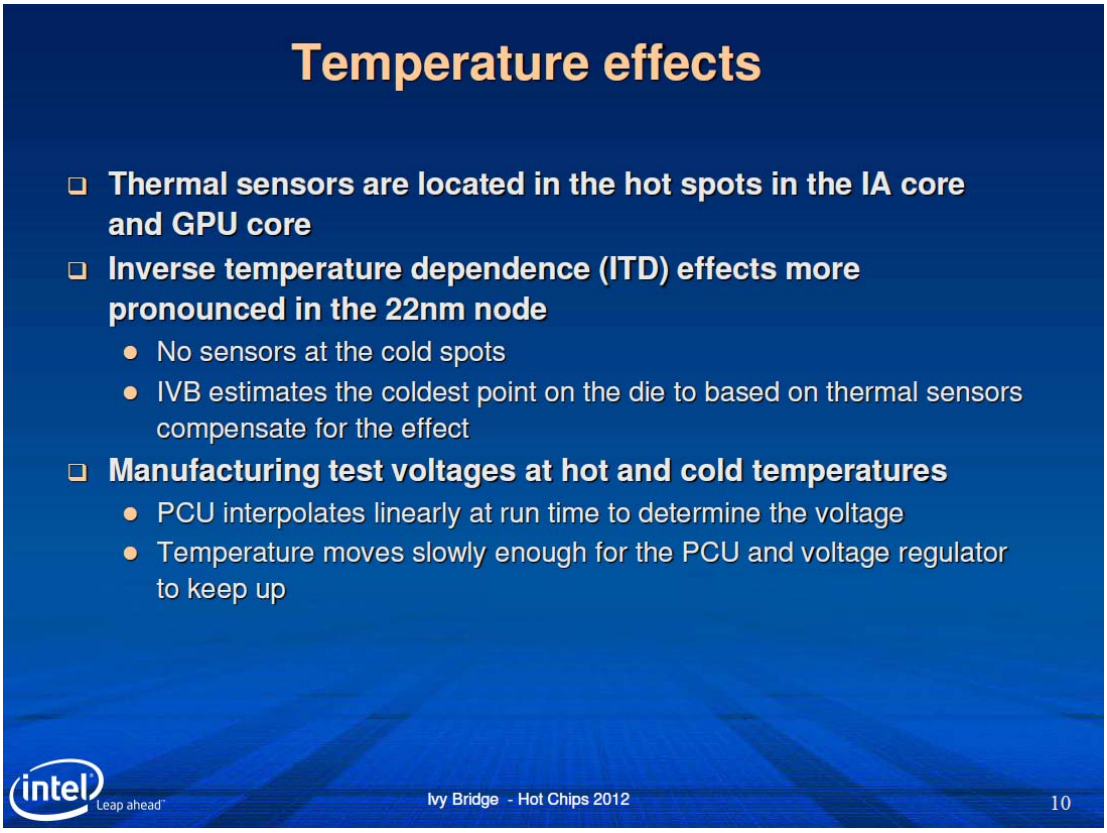


51. As a further example, public statements by Intel engineers also demonstrate that the PCU uses thermal information to adjust the power supply voltage level: "As temperature is lowered, the frequency of the chip can degrade because of the ITD effect (Inverse Temperature Dependence). In this case, information from the thermal sensor is used to raise the supply voltage to maintain performance." Dr. Peter Shor, http://www.ee.columbia.edu/compact-thermal-sensors-intel-processors-90nm-22nm.

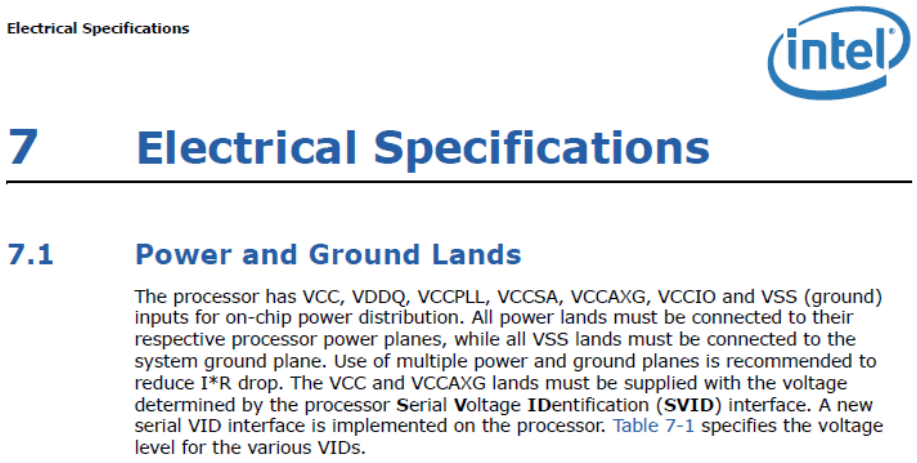
["adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit."]

52. The '027 accused products use a method that includes adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit. For example, Intel marketing materials show that the PCU adjusts a

regulation signal of a voltage regulator, a DC-to-DC converter in a manner such as that described below.



53. As a further example, Intel technical documentation such as the specification included below demonstrates that '027 accused products adjust a regulation signal to a DC-to-DC converter via interfaces such as the "processor Serial Voltage IDentification (SVID) interface."



Electrical Specifications

7 Electrical Specifications

7.1 Power and Ground Lands

The processor has VCC, VDDQ, VCCPLL, VCCSA, VCCAXG, VCCIO and VSS (ground) inputs for on-chip power distribution. All power lands must be connected to their respective processor power planes, while all VSS lands must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC and VCCAXG lands must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (**SVID**) interface. A new serial VID interface is implemented on the processor. Table 7-1 specifies the voltage level for the various VIDs.

https://www.intel.com/content/www/us/en/processors/core/3rd-gen-core-desktop-vol-1-datasheet.html at 75.

54. Intel has long had knowledge of the '027 Patent. For example, VLSI's predecessor Freescale provided notice of this patent to Intel on May 30, 2014. To the extent Intel claims it did not have broader actual knowledge of the '027 Patent, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

55. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '027 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '027 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers

directly infringe the '027 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

56. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '027 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '027 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '027 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '027 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '027 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

57. As a result of Intel's infringement of the '027 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

58. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '027 Patent.

59. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

60. VLSI is informed and believes, and thereon alleges, that the infringement of the '027 Patent by Intel has been and continues to be willful. As noted above, Intel has long had knowledge of the '027 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

61. VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

THIRD CLAIM

(Infringement of U.S. Patent No. 7,247,552)

62. VLSI re-alleges and incorporates herein by reference Paragraphs 1-61 of its Complaint.

63. The '552 Patent, entitled "Integrated circuit having structural support for a flip-chip interconnect pad and method therefor," was duly and lawfully issued July 24, 2007. A true and correct copy of the '552 Patent is attached hereto as Exhibit 3.

64. The '552 Patent names Scott K. Pozder, Kevin J. Hess, Pak K. Leung, Edward O. Travis, Brett P. Wilkerson, David G. Wontor, and Jie-Hua Zhao as co-inventors.

65. The '552 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '552 Patent, including the right to seek damages for past, current, and future infringement thereof.

66. The '552 Patent states that it "relates to packaged semiconductors and more particularly to interconnect pads of integrated circuits for making electrical connection to underlying conductive layers." Ex. 3 at 1:18-21.

67. The '552 Patent provides "a method and apparatus for providing structural support for interconnect pad locations in an integrated circuit (IC) by using novel layout techniques in the metallization and dielectric stack underlying the pad. As used herein, an interconnect pad, formed of metal, is placed at the surface of an integrated circuit where an electrical connection is made from the pad to one or more underlying interconnect layers. In a typical IC design, multiple interconnect layers separated by interlevel dielectrics are formed in a stack to provide the required interconnections between devices in the semiconductor substrate." Ex. 3 at 2:31-42.

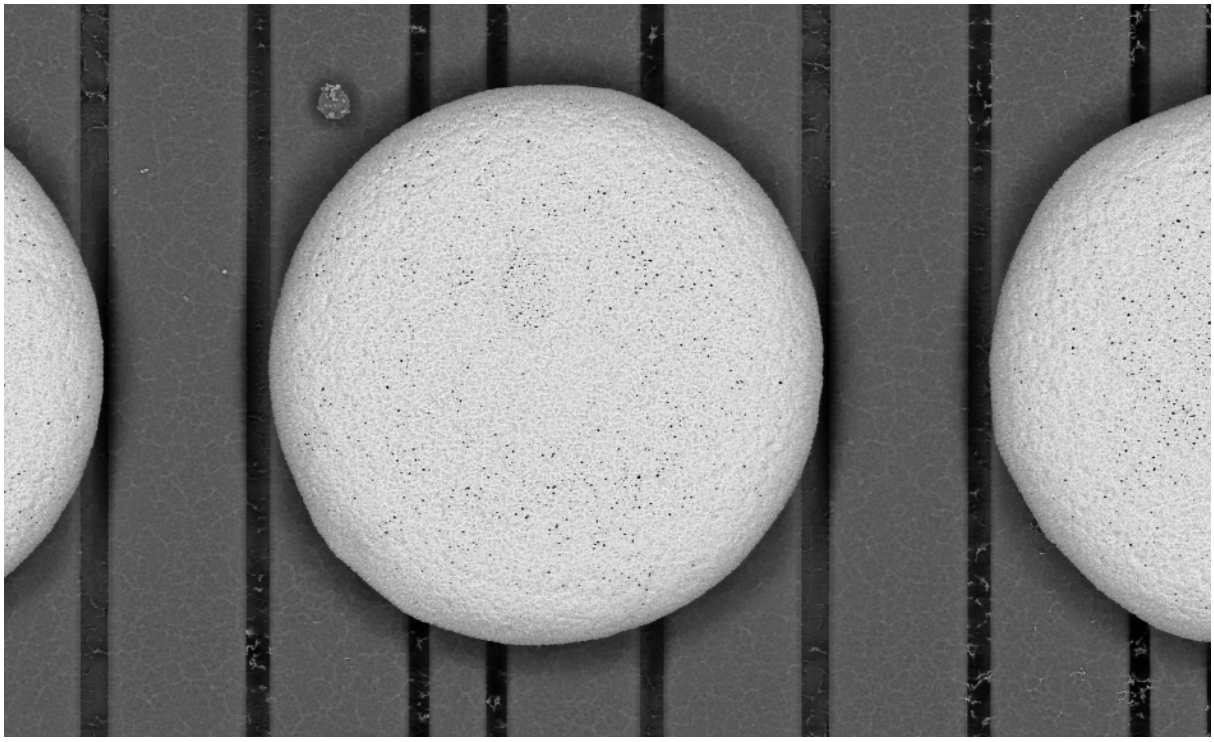
68. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '552 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products with metal dummy lines to reinforce regions under bond pads in an infringing manner.

69. The '552 accused products embody every limitation of at least claim 11 of the '552 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["A method of making an integrated circuit having a plurality of bond pads, comprising:"]

70. The '552 accused products are manufactured using a method of making an integrated circuit having a plurality of bond pads.

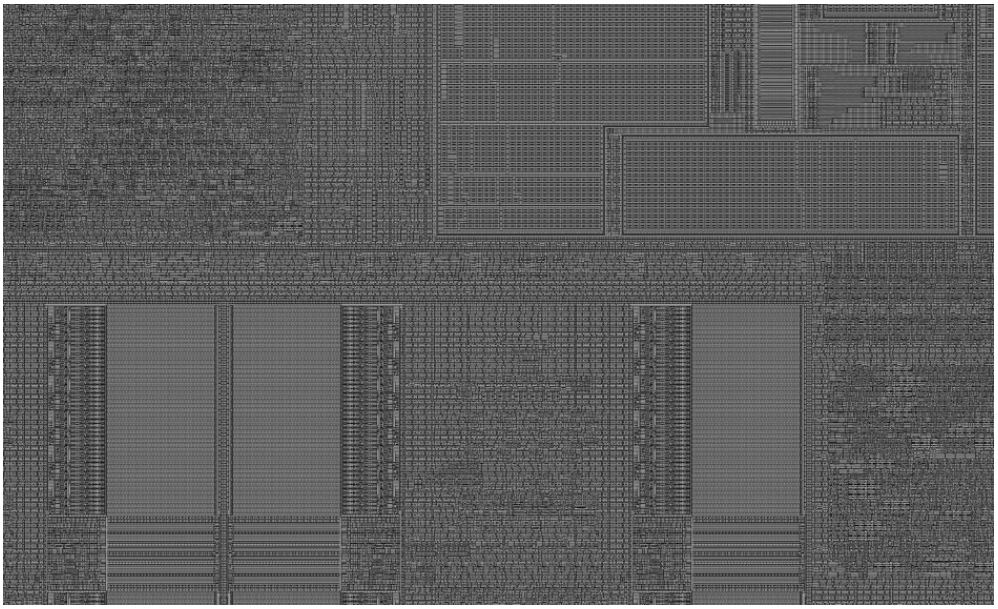
71. For example, electron micrographs of Intel products, including the i7-4770 processor, show a plurality of bond pads:



["developing a circuit design of the integrated circuit;"]

72. The '552 accused products are manufactured using a method that includes developing a circuit design of the integrated circuit.

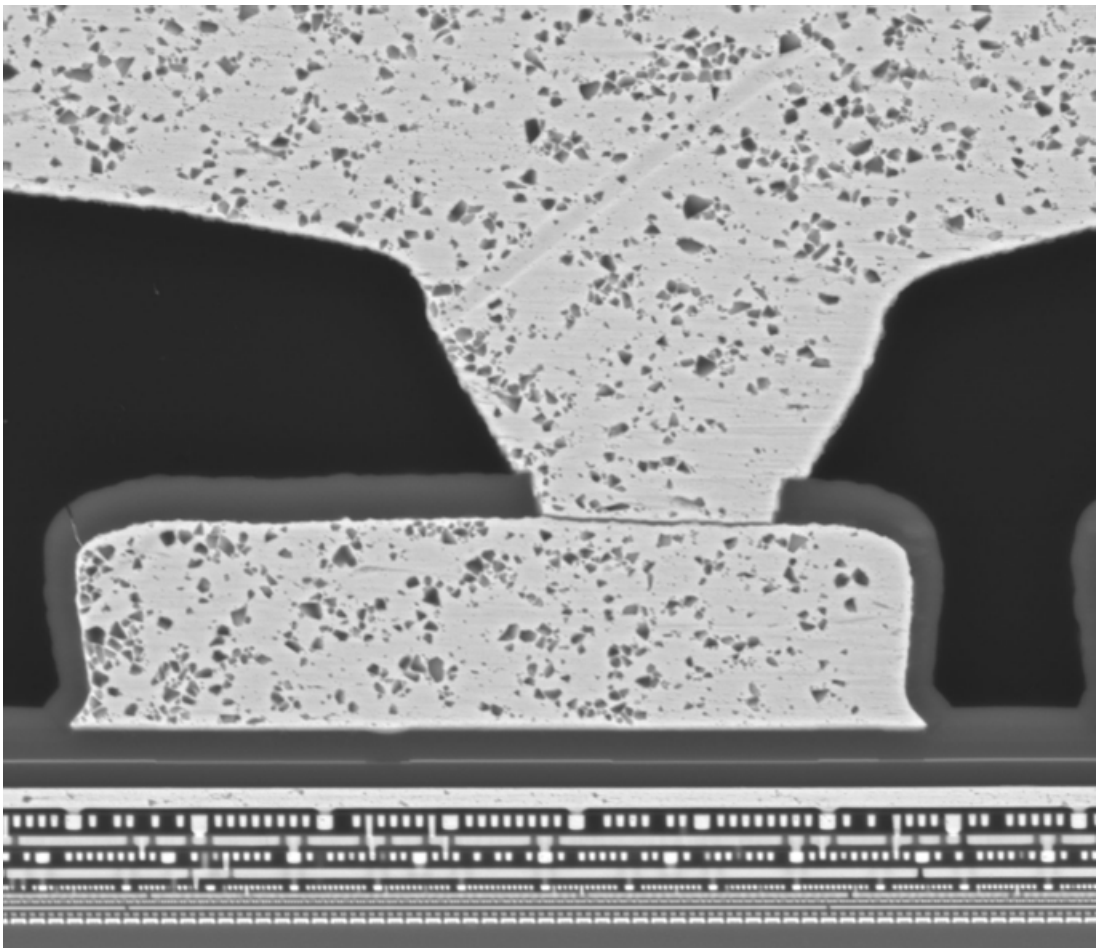
73. For example, electron micrographs of Intel products, including the i7-4770 processor, show a circuit design made up of gates and interconnecting wires:



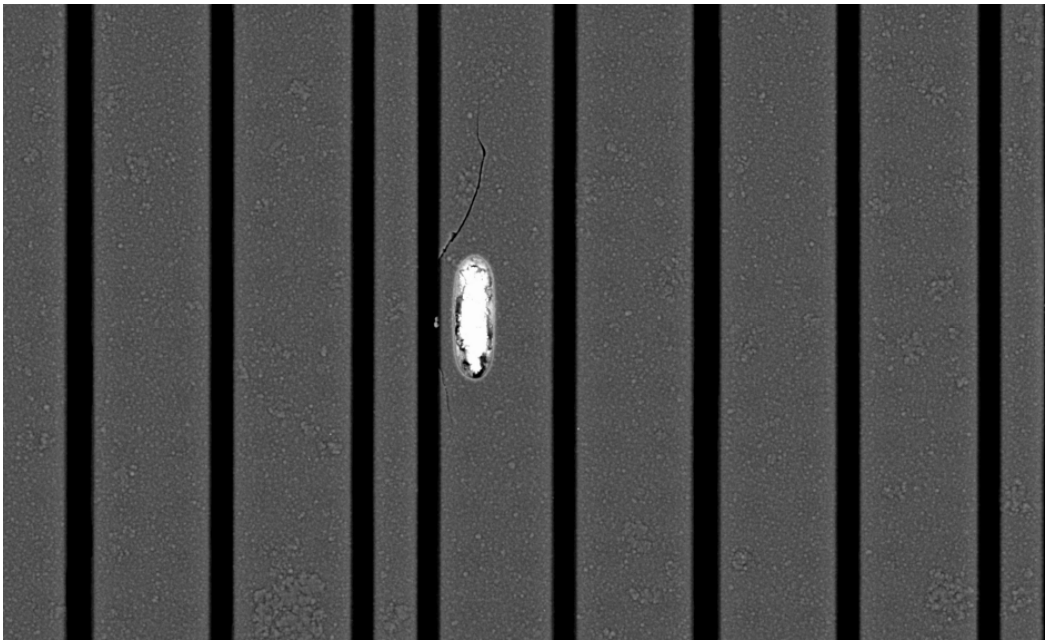
["developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of interconnect layers underlying a first bond pad of the plurality of bond pads, at least one of the plurality of interconnect layers not being electrically connected to the first bond pad and used for wiring or interconnect other than directly to the first bond pad;"]

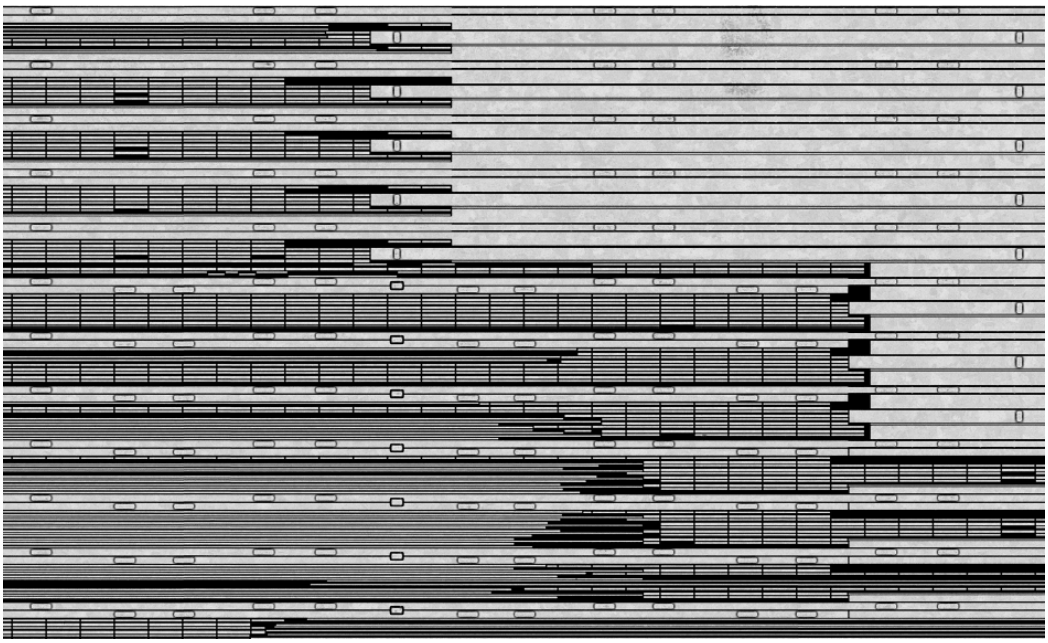
74. The '552 accused products are manufactured using a method that includes developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of interconnect layers underlying a first bond pad of the plurality of bond pads, at least one of the plurality of interconnect layers not being electrically connected to the first bond pad and used for wiring or interconnect other than directly to the first bond pad.

75. For example, electron micrographs of Intel products, including the i7-4770 processor, show several interconnect layers underlying the bond pads.



76. Some, but not all, of the interconnects on various interconnect layers are electrically connected using vias to the bond pads, in such a way that practices this element.

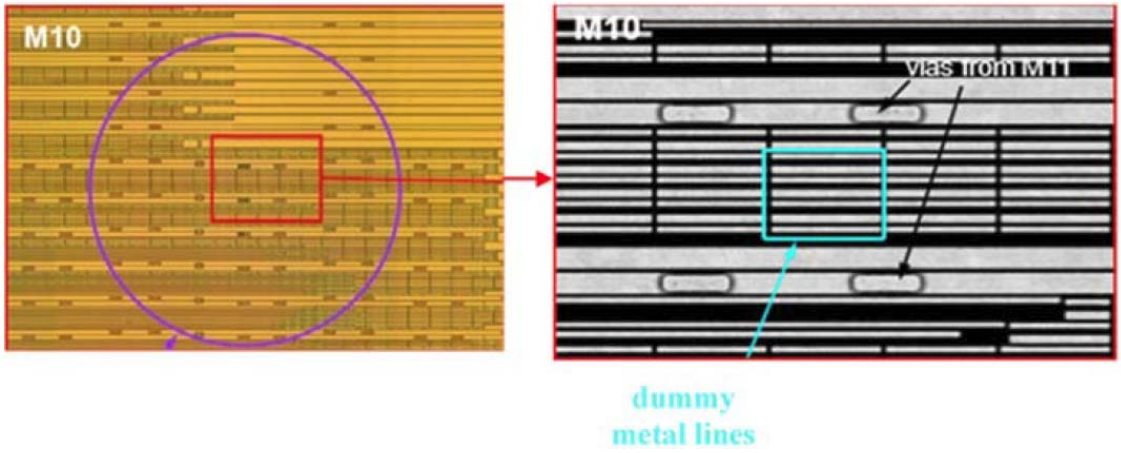




["defining a force region at least under the first bond pad of the plurality of bond pads, wherein the force region comprises a first portion of each of the plurality of interconnect layers;"]

77. The '552 accused products are manufactured using a method that includes defining a force region at least under the first bond pad of the plurality of bond pads, wherein the force region comprises a first portion of each of the plurality of interconnect layers.

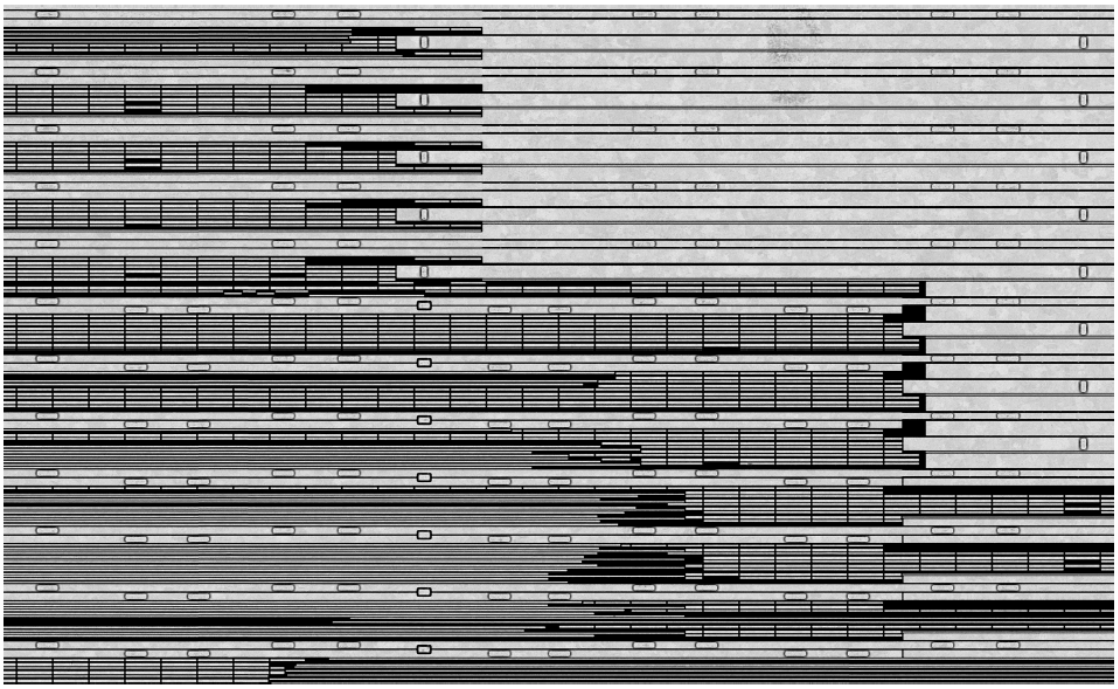
78. For example, electron micrographs of Intel products, including the i7-4770 processor, show a region under each bond pad that represents a "force region," in a manner such as that shown below.



["identifying a first interconnect layer of the plurality of interconnect layers in which the first portion of the first interconnect layer has a metal density below a predetermined percentage;"]

79. The '552 accused products are manufactured using a method that includes identifying a first interconnect layer of the plurality of interconnect layers in which the first portion of the first interconnect layer has a metal density below a predetermined percentage.

80. For example, electron micrographs of Intel products, including the i7-4770 processor, show that particular interconnect layers have regions where the density of actively used metal is low.



["modifying the layout by adding dummy metal lines to the first portion of the first interconnect layer to increase the metal density of the first portion of the first interconnect layer; and"]

81. The '552 accused products are manufactured using a method that includes modifying the layout by adding dummy metal lines to the first portion of the first interconnect layer to increase the metal density of the first portion of the first interconnect layer.

82. For example, electron micrographs of Intel products, including the i7-4770 processor, show that dummy metal lines have been added to the particular interconnect layers in regions where the density of actively used metal is low through a process that practices this element.

["making the integrated circuit comprising the dummy metal lines."]

83. The '552 accused products are manufactured using a method that includes making the integrated circuit comprising the dummy metal lines. For example, the above discussion provides an example of how the integrated circuit comprising the dummy metal lines is made.

84. Intel has had knowledge of the '552 Patent at least since the filing of this complaint, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the '552 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

85. As a result of Intel's infringement of the '552 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

86. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '552 Patent.

87. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

88. VLSI is informed and believes, and thereon alleges, that Intel's infringement of the '552 Patent has been and continues to be willful.

89. VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

FOURTH CLAIM

(Infringement of U.S. Patent No. 7,523,331)

90. VLSI re-alleges and incorporates herein by reference Paragraphs 1-89 of its Complaint.

91. The '331 Patent, entitled "Power saving operation of an apparatus with a cache memory," was duly and lawfully issued April 21, 2009. A true and correct copy of the '331 Patent is attached hereto as Exhibit 4.

92. The '331 Patent names Gerardus Wilhelmus Theodorus Van Der Heijden as the inventor.

93. The '331 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '331 Patent, including the right to seek damages for past, current, and future infringement thereof.

94. The '331 Patent "relates to an apparatus that supports a low power operating mode." Ex. 4 at 1:4-5.

95. The '331 Patent explains that "[a]mong others it is an object of the invention to provide a reduction of power consumption by an apparatus with a low power operating mode." Ex. 4 at 1:50-52.

96. The '331 Patent further explains that "at least part of a cache memory is selectively kept active in the low power mode while the main memory is deactivated (deactivation typically comprising cutting power supply to the main memory, or at least significantly reducing power supply consumption, so that the main memory is not or not fully operational). Prior to switching to the low power mode a program of instructions that are needed to perform a function while the apparatus is in the low power mode is loaded into the cache memory for later use. When an instruction processing circuit performs the function in the low power mode, it loads the instructions from the cache memory, without activating (supplying full power) the main memory." Ex. 4 at 1:54-66.

97. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '331 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that include an infringing Management Engine and a CPU that includes a memory controller.

98. The '331 accused products embody every limitation of at least claim 7 of the '331 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["A method of operating an apparatus that contains an instruction processing circuit, a main memory addressable by the instruction processing circuit and a cache memory, the method comprising:"]

99. The '331 accused products operate using a method of operating an apparatus that contains an instruction processing circuit, a main memory addressable by the instruction processing circuit and a cache memory.

100. For example, documentation written by Intel engineers explains that the Management Engine ("ME") "hardware is comprised of a processor, code and data caches, DMA (direct memory access) engines, cryptography engines, read-only memory (ROM), internal memory (static random-access memory, or SRAM), a timer, and other supporting devices." https://link.springer.com/book/10.1007%2F978-1-4302-6572-6 at 30.

["using the cache memory and the main memory in a normal operating mode, to cache in cache memory a part of data and/or instructions that the instruction

processing circuit addresses in the main memory during execution, and to substitute cached data and/or instructions when the instruction processing circuit addresses the data and/or instructions in the main memory;"]

101. The '331 accused products operate using the cache memory and the main memory in a normal operating mode, to cache in cache memory a part of data and/or instructions that the instruction processing circuit addresses in the main memory during execution, and to substitute cached data and/or instructions when the instruction processing circuit addresses the data and/or instructions in the main memory.

102. For example, documentation written by Intel engineers explains that "[t]here is a small code and data cache to help the processor reduce the number of accesses to the internal SRAM. The internal SRAM is the memory that stores firmware code and data at runtime. The capacity of SRAM varies depending on the product, but generally ranges between 256KB and 1MB. In addition to the internal SRAM, the management engine also uses a certain amount of DRAM (dynamic random-access memory) from the main system memory. Code and data pages that are not recently accessed may be evicted from the SRAM and swapped out to the reserved memory. When a page is needed again, it will be swapped in to the SRAM." https://link.springer.com/book/10.1007%2F978-1-4302-6572-6 at 30-31.

["storing, in the main memory, a program of instructions for executing an interrupt function during operating in a low power operating mode, wherein the interrupt program is stored at addresses in main memory that have been selected so that all instructions of the interrupt program can be stored together in the cache memory;"]

103. The '331 accused products operate by storing, in the main memory, a program of instructions for executing an interrupt function during operating in a low power operating mode,

wherein the interrupt program is stored at addresses in main memory that have been selected so that all instructions of the interrupt program can be stored together in the cache memory.

104. For example, documentation written by Intel engineers shows that the Intel Management Engine uses an interrupt controller.

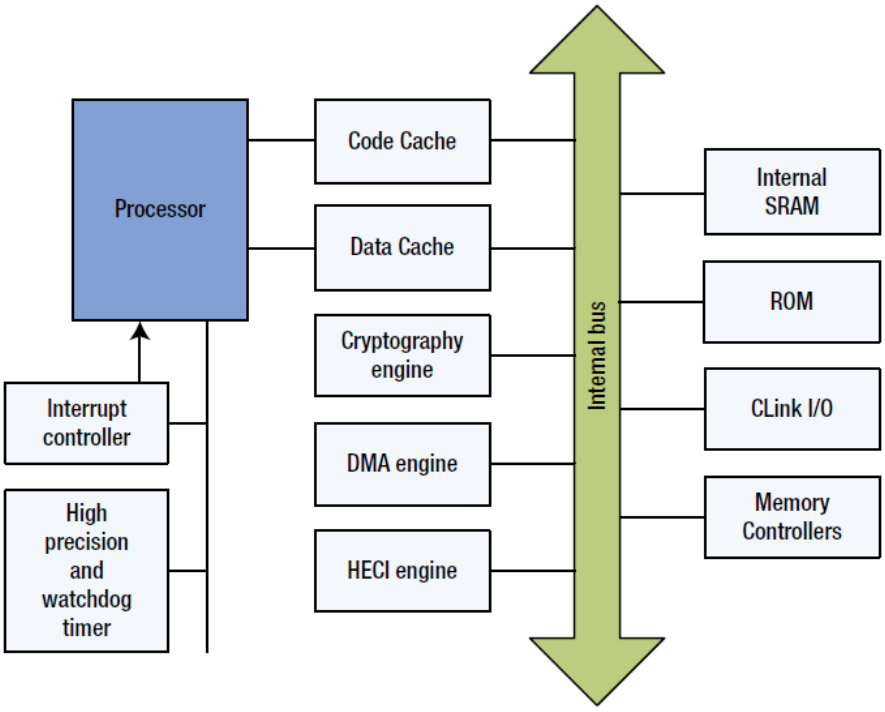


Figure 2-1. *Hardware architecture of the management engine*

https://link.springer.com/book/10.1007%2F978-1-4302-6572-6 at 30.

105. As explained above, the ME stores code in both internal cache as well as system main memory through a process that practices this element. For example, upon information and belief, the ME stores, in the main memory, a program of instructions for executing an interrupt function during operating in a low power operating mode, wherein the interrupt program is stored at addresses in main memory that have been selected so that all instructions of the interrupt program can be stored together in the cache memory.

["detecting that it is no longer necessary to operate in the normal operating mode; switching to the low power operating mode once it is detected that it is no longer necessary to operate in the normal operating mode, by"]

106. The '331 accused products operate by detecting that it is no longer necessary to operate in the normal operating mode and switching to the low power operating mode once it is detected that it is no longer necessary to operate in the normal operating mode.

107. For example, Intel technical documentation explains that systems including the Intel Management Engine switch to ACPI system states based on detection of signals from the operating system, including the S5 state, in a manner such as that described below.

Power Management

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

https://www.intel.com/content/www/us/en/processors/core/3rd-gen-core-desktop-vol-1-datasheet.html at 48.

["loading the interrupt program into the cache memory from the main memory, wherein all instructions of the interrupt program are stored together in the cache memory;"]

108. The '331 accused products operate by loading the interrupt program into the cache memory from the main memory, wherein all instructions of the interrupt program are stored together in the cache memory.

109. For example, documentation written by Intel engineers, including the example provided below, explains that the Management Engine remains on during the S5 system state, even though the CPU and main memory are turned off.

3.4.3.1 Intel® ME ON in Host Sleep States

Under Intel ME Power Control,

1. Select 'Intel ME ON in Host Sleep States'.
2. Press Enter to select.

The following options can be selected:

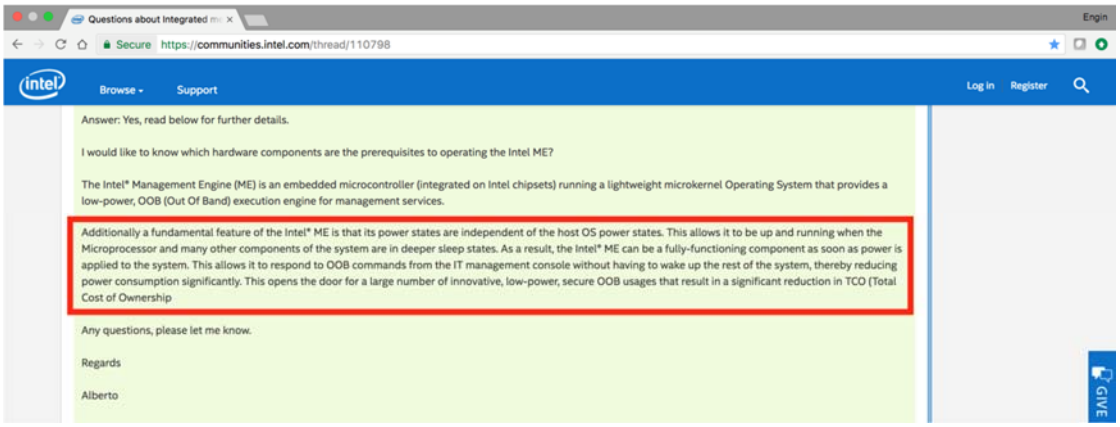
- **Desktop: On in S0** – Power Package 1
- **Desktop: On in S0, ME Wake in S3, S4-5** –Power Package 2*

Table 1: Supported Power Packages

Power Package	1	2*
S0	ON	ON
S3	OFF	ON /ME WoL
S4/S5	OFF	ON/ ME WoL

*Default setting

https://www.intel.com/content/dam/support/us/en/documents/motherboards/desktop/db75en/sb/intel_mebx_user_guide_for_db75en.pdf at 18.



https://communities.intel.com/thread/110798.

110. Upon information and belief, the ability to run code at the ME regardless of the power state of main memory means that these systems function by loading the interrupt program into the cache memory from the main memory, wherein all instructions of the interrupt program are stored together in the cache memory.

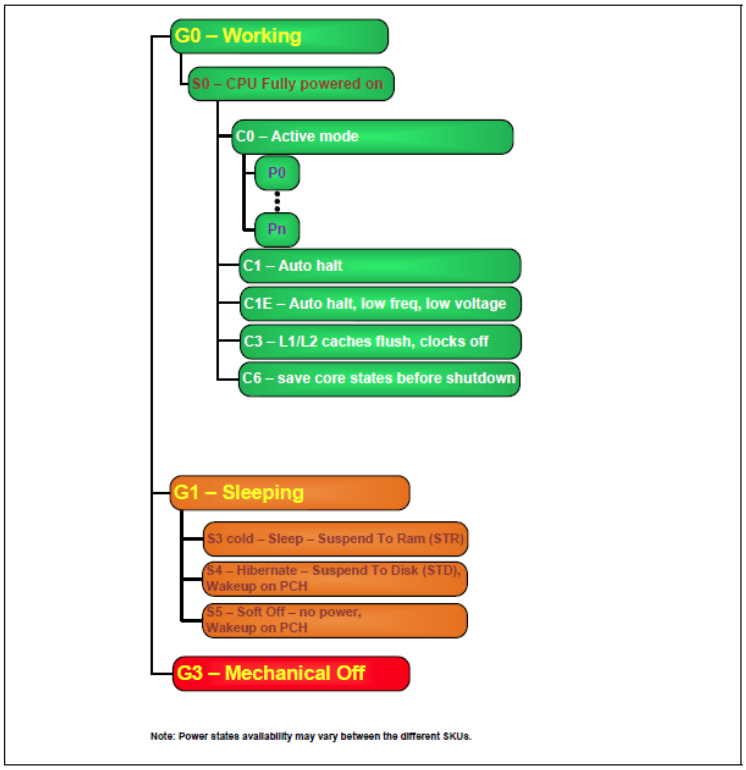
["deactivating the main memory to reduce power consumption, but keeping active at least a part of the cache memory, that is needed for retrieving the interrupt program and for executing the interrupt function; executing the interrupt program from said at least part of the cache memory."]

111. The '331 accused products operate by deactivating the main memory to reduce power consumption, but keeping active at least a part of the cache memory, that is needed for retrieving the interrupt program and for executing the interrupt function and executing the interrupt program from said at least part of the cache memory.

112. For example, documentation written by Intel engineers explains that the S5 power state is a deeper power state than S4, the "Suspend to Disk" power state wherein the contents of main memory is flushed, and all power (including main memory) is "lost." However, upon

information and belief, at least a part of the cache memory must be kept active for retrieving and executing the interrupt function through a process that practices this element.

Figure 4-1. Processor Power States



https://www.intel.com/content/www/us/en/processors/core/3rd-gen-core-desktop-vol-1-datasheet.html at 47.

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State	Description
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G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

Id. at 48.

113. Intel has long had knowledge of the '331 Patent. For example, the '331 Patent has been cited in Intel patent prosecutions, including during the prosecution of its U.S. Patent No. 7,523,327. To the extent Intel claims it did not have broader actual knowledge of the '331 Patent, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

114. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '331 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software

developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '331 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '331 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

115. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '331 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '331 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '331 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '331 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '331 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

116. As a result of Intel's infringement of the '331 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

117. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '331 Patent.

118. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

119. VLSI is informed and believes, and thereon alleges, that the infringement of the '331 Patent by Intel has been and continues to be willful. As noted above, Intel has long had knowledge of the '331 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

120. VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

FIFTH CLAIM

(Infringement of U.S. Patent No. 8,081,026)

121. VLSI re-alleges and incorporates herein by reference Paragraphs 1-120 of its Complaint.

122. The '026 Patent, entitled "Method for supplying an output supply voltage to a power gated circuit and an integrated circuit," was duly and lawfully issued December 20, 2011. A true and correct copy of the '026 Patent is attached hereto as Exhibit 5.

123. The '026 Patent names Sergey Sofer, Eyal Melamed-Kohen, and Valery Neiman as co-inventors.

124. The '026 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '026 Patent, including the right to seek damages for past, current, and future infringement thereof.

125. The '026 Patent states that it "relates to a method for supplying an output supply voltage to a power gated circuit and to an integrated circuit that has a power gated circuit." Ex. 5 at 1:7-9.

126. The '026 Patent explains that "[i]ntegrated circuits can be required to operate at a certain speed and to consume up to an allowable level of current. These contradicting demands can reduce the yield of the manufacturing process—as some integrated circuits can be too slow but comply to the current consumption requirements whilst some integrated circuits will exhibit a too high current consumption but comply with the speed requirements." Ex. 5 at 1:34-40.

127. The '026 Patent further explains that "[i]n case the power gated circuit 30 has to be in a low power mode, also referred to as gated mode, the conductivity of the power gating switch can be set to a level that facilitates a power retention mode that is power efficient and enables memory and latch devices that belong to the power gated circuit to retain data. Retention mode is the low power mode when the integrated circuit does not perform any operation, and only retains data stored in memory or latch devices." Ex. 5 at 3:12-19.

128. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '026 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that supply an output supply voltage to a power gated circuit in an infringing manner.

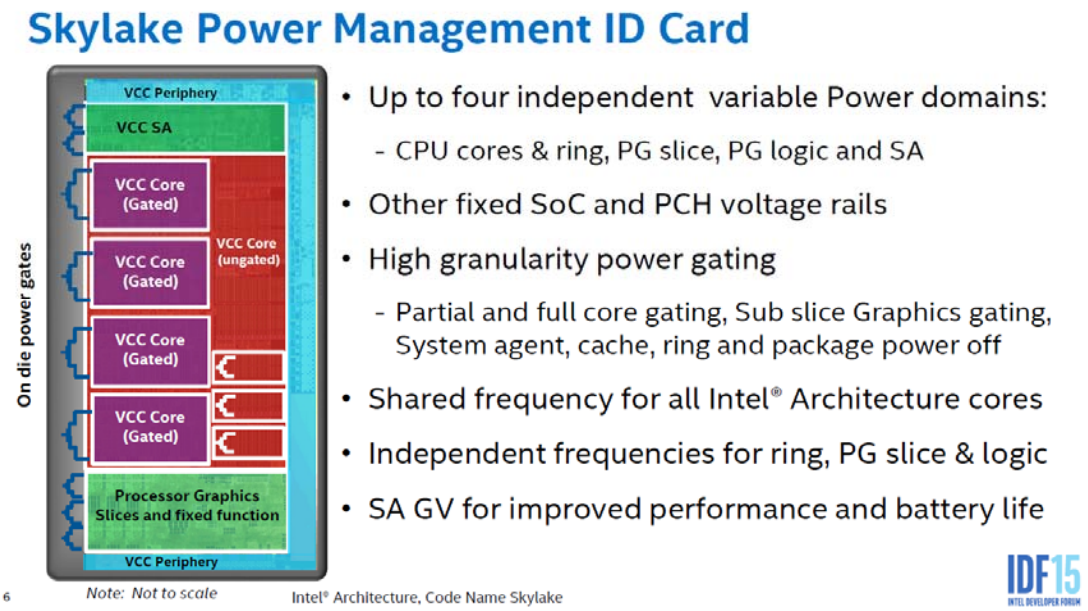
129. The '026 accused products embody every limitation of at least claim 13 of the '026 Patent, literally or under the doctrine of equivalents, as set forth below. The further

descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["A method for supplying an output supply voltage to a power gated circuit, the method comprising"]

130. The '026 accused products use a method for supplying an output supply voltage to a power gated circuit.

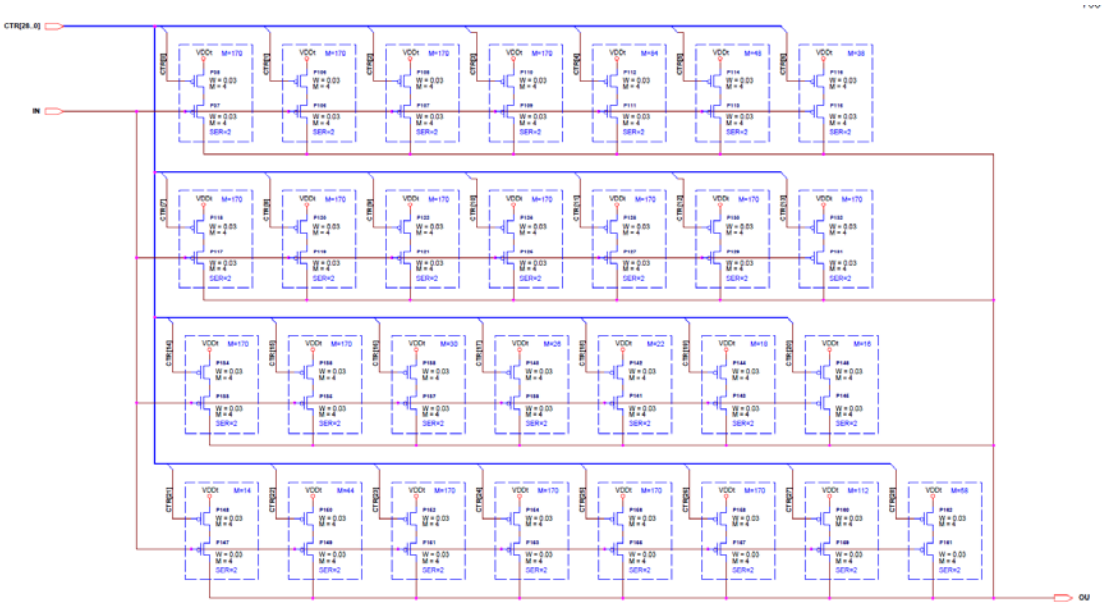
131. For example, Intel marketing materials show various power gated circuits with independent power gates supplying output supply voltages. One example is provided below.



["providing to an input port of a power gating switch an input supply voltage;"]

132. The '026 accused products use a method that includes providing to an input port of a power gating switch an input supply voltage.

133. For example, reverse engineering of the Intel i3-6300 shows that the power gating switch receives an input supply voltage:



["receiving, by a control circuit, a mode indicator that indicates of a desired mode of the power gated circuit;"]

134. The '026 accused products use a method that includes receiving, by a control circuit, a mode indicator that indicates of a desired mode of the power gated circuit.

135. For example, technical documentation shows that the products receive at control circuitry, including the PCU, a mode indicator that indicates a desired mode, such as the Processor IA core C6 state, in a way such as that described below.

> **Processor IA core C6 State**
>
> Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

https://www.intel.com/content/www/us/en/processors/core/desktop-6th-gen-core-family-datasheet-vol-1.html at 66.

["receiving, by the control circuit, a leakage indicator that indicates of a leakage level of the power gated circuit;"]

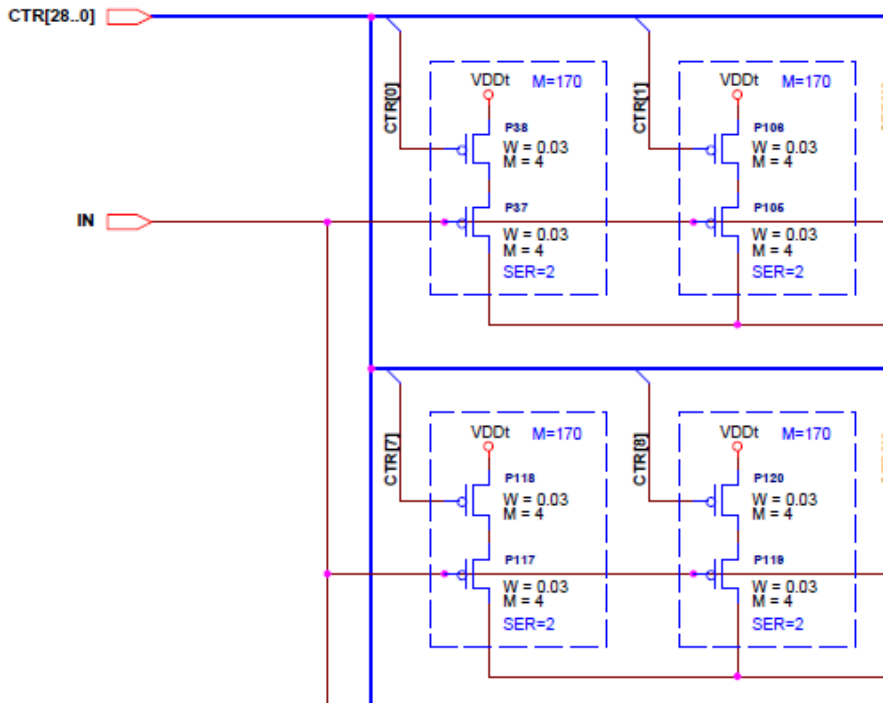
136. The '026 accused products use a method that includes receiving, by the control circuit, a leakage indicator that indicates of a leakage level of the power gated circuit.

137. For example, Intel engineers have confirmed that control circuitry, including the PCU, receive indication of the leakage level of the power gated circuit by a process that practices this element. *See, e.g.*, http://myeventagenda.com/sessions/0B9F4191-1C29-408A-8B61-65D7520025A8/7/5#sessionID=155 ("Sure temperature is always there, leakage is a function of temperature, we calculate the leakage at run time and we do all of the optimizations based on the temperature and the leakage.").

["selecting, by the control circuit, a value of a control signal based on the mode indicator and on the leakage indicator; supplying the control signal to a control port of the power gating switch"]

138. The '026 accused products use a method that includes selecting, by the control of a control signal based on the mode indicator and on the leakage indicator, and supplying the control signal to a control port of the power gating switch.

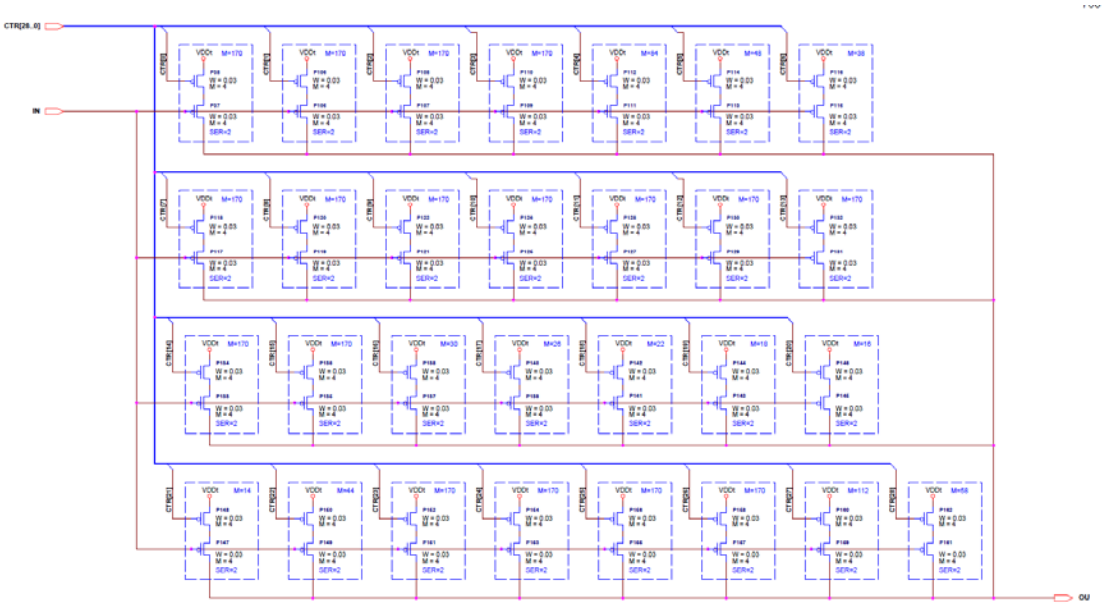
139. For example, as discussed above, control circuitry including the PCU, receive both a mode indicator and a leakage indicator in a manner such as that shown below. In one such embodiment, this circuitry is then connected to a control port of the power gating switch shown here as CTR[28:0]:



["providing, from an output port of the power gating switch, the output supply voltage to the power gated circuit; wherein a relationship between a value of the input supply voltage and a value of the output supply voltage is responsive to the value of the control signal."]

140. The '026 accused products use a method that includes providing, from an output port of the power gating switch, the output supply voltage to the power gated circuit; wherein a relationship between a value of the input supply voltage and a value of the output supply voltage is responsive to the value of the control signal.

141. For example, the value of the control signal determines the number of power gating transistors that are active, passing current from the input to the output port of the power gating switch. This number determines the resistance across the gate, and therefore the relationship between the voltage at the input and the voltage of the output, using architecture such as that shown below.



142. Intel has long had knowledge of the '026 Patent. For example, the '026 Patent has been cited in Intel patent prosecutions, including during the prosecution of its U.S. Patent No. 8,810,304. To the extent Intel claims it did not have broader actual knowledge of the '026 Patent, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

143. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '026 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '026 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers

directly infringe the '026 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

144. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '026 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '026 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '026 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '026 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '026 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

145. As a result of Intel's infringement of the '026 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

146. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '026 Patent.

147. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

148. VLSI is informed and believes, and thereon alleges, that the infringement of the '026 Patent by Intel has been and continues to be willful. As noted above, Intel has long had knowledge of the '026 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

149. VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, VLSI prays for judgment against Intel as follows:

A. That Intel has infringed, and unless enjoined will continue to infringe, each of the Asserted Patents;

B. That Intel has willfully infringed each of the Asserted Patents;

C. That Intel pay VLSI damages adequate to compensate VLSI for Intel's infringement of the Asserted Patents, together with interest and costs under 35 U.S.C. § 284;

D. That Intel be ordered to pay prejudgment and postjudgment interest on the damages assessed;

E. That Intel pay VLSI enhanced damages pursuant to 35 U.S.C. § 284;

F. That Intel be ordered to pay supplemental damages to VLSI, including interest, with an accounting, as needed;

G. That Intel be enjoined from infringing the Asserted Patents, or if its infringement is not enjoined, that Intel be ordered to pay ongoing royalties to VLSI for any postjudgment infringement of the Asserted Patents;

H. That this is an exceptional case under 35 U.S.C. § 285, and that Intel pay VLSI's attorneys' fees and costs in this action; and

I. That VLSI be awarded such other and further relief, including equitable relief, as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), VLSI hereby demands a trial by jury on all issues triable to a jury.

Dated: June 28, 2018

Respectfully submitted,

FARNAN LLP

/s/ Brian E. Farnan

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